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Atomic Layer Epitaxy of Advanced Devices and Circuits

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For advanced electron devices, atomic layer epitaxy offers two capabilities which no other semiconductor growth technique provides: monolayer thickness control and conformal over-growth. Monolayer thickness control was used to ensure lateral and vertical uniformity for devices incorporating quantum wells and tunnel barriers, e.g. resonant tunneling diodes/over large area substrates. Conformal overgrowth was used for device passivation and in quantum well structures embedded in groves under sidewalls. ALE was also used and showed definite advantages over other growth techniques in several other areas such as planar and carbon doping, high quality interfaces and selective area epitaxy. During the last three years we have addressed the major challenges facing the ALE technique, improved the material quality for both binary and ternary alloy III-V compounds and then applied the ALE technique to several device structures, such as Resonant tunneling diodes, planar doped FETs and Bipolar junction transistors.

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Summary of Major Achievements

I-1. ALE Growth Facilities:

Two new ALE reactors are currently operational. The first is home built and is adequate for 1.8 x 1.8 cm size substrates. The second is a modified Emcore reactor capable of three 2" wafers. Both reactors operate near atmospheric pressure with a growth rate of about 0.5 μm/h. The ultra-high vacuum "Riber" system is installed, and is currently operational.

I.2. Material Development

- Device quality GaAs, InGaAs and GaInP layers with carbon background doping of less than 10^{15}/cm^3 were achieved. ALE growth of p-type AlGaAs with carrier concentrations in the range 10^{17}-10^{20}/cm^3 was also achieved. Sidewall and selective area epitaxy was developed.

- Device quality GaAs by laser assisted ALE (LALE) and laser assisted chemical vapor deposition (LCVD) was developed.

I.3. Device Demonstrations

Progress has been primarily in heterojunction development and initial device demonstrations. Highlights of this are as follows:

- pin junctions with low leakage current and pin junctions in trenches with very low leakage current were achieved.

- pinip storage capacitor with high storage time was demonstrated.

- ALE MESFET with equivalent dc and rf parameters to MBE MESFETs (gm = 187 mS/mm, f_T = 27 GHz) was achieved.

- δ-doped MESFETs have shown a transconductance as high as 347 mS/mm for a 0.5 μm gate length device.

- δ-doped FET with sidewall source and drain were demonstrated.

- Good n^{++} overgrowth on MESFET structure was achieved.

- The first ALE pnp bipolar transistor with a current gain of 120 at Ic = 500 A/cm^2 was achieved.

- Selective overgrowth on patterned GaAs was demonstrated.

- InGaP/GaAs and AlGaAs/GaAs quantum wells exhibiting red-shifted quantum well photoluminescence were developed.

- The first ALE resonant tunneling diode in AlGaAs/GaAs system with 77 K° peak-to-valley current density of 1.3 was achieved.

- A DCAM Circuit was demonstrated.

- pin detector and δ-doped FETs were selectively grown by laser assisted ALE/CVD.

This report describes, in detail, the activities carried out (1988-1990) by N. C. State University, Texas Instruments and Purdue University and can be outlined by three major tasks:

- Material Development and Discrete Devices
- Advanced Devices and Circuits
- Dynamic Content Addressable Memory

1. Materials Developments and Discrete Devices

1.1 Introduction

For advanced electron devices, atomic layer epitaxy offers two capabilities which no other semiconductor growth technique provides: monolayer thickness control and conformal over-growth. Monolayer thickness control is important to ensure lateral and vertical uniformity for devices incorporating quantum wells and tunnel barriers, e.g. resonant tunneling diodes/transistors and quantum-well lasers. Conformal overgrowth can be used for device passivation or isolation storage capacitance and for a variety of high density digital and low parasitic microwave device structures. In addition, it may allow the interconnection of elemental electron devices such as quantum dots. ALE also offers definite advantages over other growth techniques in several other areas such as planar and carbon doping, high quality interfaces and selective area epitaxy.

During the last three years we have addressed the major challenges facing the ALE technique, improved the material quality for both binary and ternary alloy III-V compounds and then applied the ALE technique to several device structures.

1.2 Current Challenges Facing the ALE Technique

The ALE technique has suffered from several shortcomings that we believe has slowed down its potential applications and the interest of many researchers.[1-2] The first problem is the very low growth rates where in some cases growth rate as slow as 0.02μm/hour were reported.[3] Some recent improvement in the growth rate was achieved and a growth rate of

about 0.1μm/h was reported,[4] which we still believe to be discouragingly slow. The main reason for such a low growth rate is the commonly used approach that is based on exposure/purging each of the reactants with a vent/run manifold configuration. The finite gas residence time in the reactor and valve switching times will always lead to the growth of only a few fractions of a micron per hour. The approach we adopted in our laboratory[6] relies on rotating the substrate between the different source gas streams that are continuously flowing through a specially designed vertical reactor. The growth rate will depend on the substrate rotation speeds. Growth rates in the range of 0.4 to 0.7μm/h can be achieved with this approach. Such growth rates are comparable with that reported by MBE. A schematic of the growth process is shown in Figure 1.
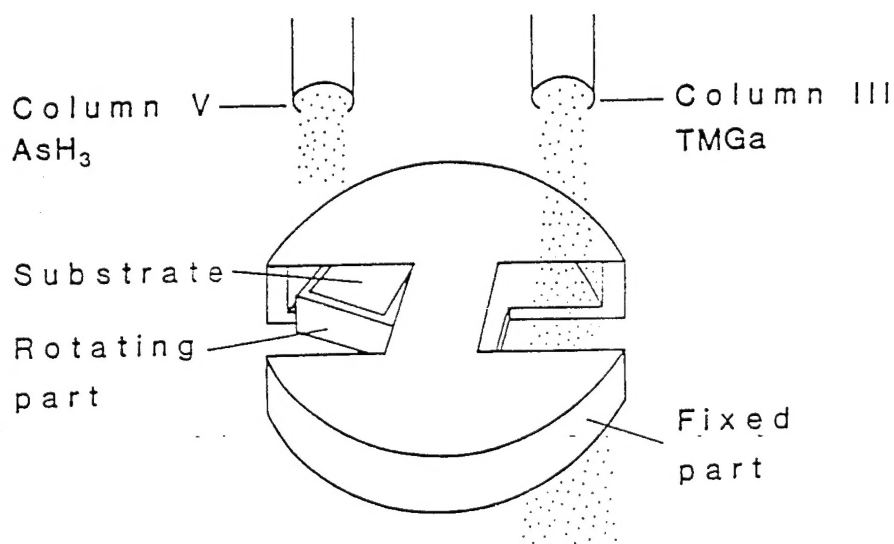

Figure 1 Schematic of the rotating susceptor for ALE.

The second problem facing ALE of III-V compounds is the high carbon background in the ALE grown films. Recently,[7] undoped GaAs with background electron concentrations in the high $10^{14}/cm^3$ to low $10^{15}/cm^3$ was achieved in our laboratory with liquid nitrogen mobility of about 30,000 $cm^2/V-sec.$, which is reasonably adequate for several devices. The device quality GaAs films were achieved by optimizing growth conditions such as growth temperature, flux of reactants and exposure times. Thus, we believe that at least for GaAs the ALE technique can provide films with convenient growth rates and good

electrical properties.

Another problem facing ALE is the synthesis of ternary alloys such as AlGaAs and InGaAs that will provide a heterostructure with different binary compounds. The problem with ternary alloys is the lack of compatible group III precursors that will adhere to the self-limiting process at the same growth temperature.[8] However, we have recently reported the growth of AlGaAs and InGaP that are both lattice matched to GaAs substrate. ALE growth of these two ternary alloys was achieved over fairly narrow conditions, and will be addressed in more detail later in this paper. Conversely, it was also found that alloys with two group V elements such as GaAsP had a fairly broad range of growth conditions.

1.3 ALE OF TERNARY ALLOYS

3.1 AlGaAs[9]

Trimethylgallium (TMGa), trimethylaluminum (TMA) and arsine (AsH$_3$, 10% in H$_2$), were the source materials. The TMGa and TMA bubblers were kept at $-10°C$ and $17°C$, respectively. The ALE growth cycle consisted of the simultaneous exposure of the substrate to the TMGa and TMA fluxes followed by a rotation to the AsH$_3$ side to complete one cycle. The substrate made one complete rotation in 2.6 sec, allowing an exposure time of about 0.3 sec for each gas stream and yielding a growth rate of about 0.4 μm/h. The composition of the ALE grown Al$_x$Ga$_{1-x}$As is controlled by the $\dfrac{TMA}{TMA+TMGa}$ molar ratio in the column III stream. We have also used the same reactor to grow AlGaAs films by the conventional MOCVD approach. In this case, the substrate is stationary and is exposed simultaneously to the TMGa, TMA and AsH$_3$ fluxes. AlGaAs films with thicknesses of about 0.8μm and 3μm for ALE and MOCVD, respectively, were grown.

The growth conditions that allow the deposition of a monolayer of AlGaAs in a self-limiting fashion in the temperature range 550−700°C were first determined. The as-grown Al$_x$Ga$_{1-x}$As films ($0 < x < 0.4$) have mirror-like surfaces. The thickness dependence of the deposited ALE films per growth cycle on the sum of TMGa+TMA moles in the column III stream is shown in Figure 2. Two values for the gas phase molar ratio, $\dfrac{TMA}{TMA+TMGa}$, 0.074 and 0.123, were studied. This gas phase composition resulted in solid compositions, x of about 0.22 and 0.33, respectively. As shown in Figure 2, the monolayer growth of Al$_{0.22}$Ga$_{0.78}$As and Al$_{0.33}$Ga$_{0.67}$As was only observed in a fairly narrow range of column III total flux. The flux range in which the deposition process becomes self-limiting is about the

same as for the 550 - 700°C growth temperature range. For higher total column III flux (> 0.075 μ mole/cycle), the growth rate began to resemble that of conventional MOCVD, where the thickness of the deposited films was doubled by doubling the total column III flux.
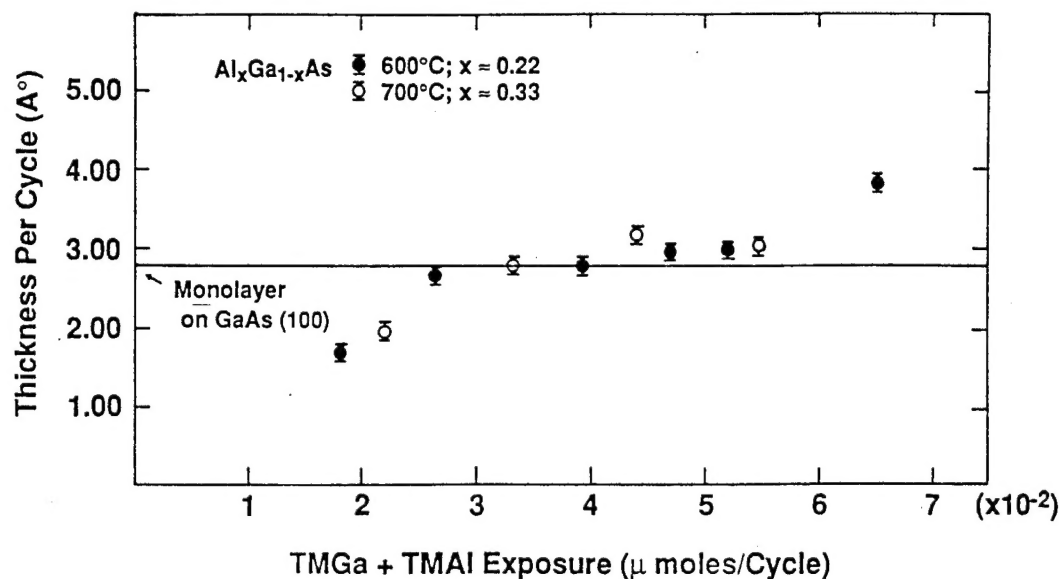

Figure 2 Thickness per ALE cycle of AlGaAs vs. (TMGa + TMA) flux.

Results shown in Figure 2 may require a reconsideration of the self-limiting mechanism, which is believed to be controlled by the surface adsorption processes of column III. For example, ALE in GaAs is believed to result from Ga species adsorbed on the surface to form a monolayer coverage, leading to very small decomposition efficiency of any additional TMGa molecules.[1] Thus, these additional TMGa molecules may re-evaporate before they decompose at the surface. For AlGaAs, if the same mechanism is present, a monolayer of mixed Ga and Al species will be formed and thus expected to prevent any further dissociation of either TMA or TMGa molecules. Therefore, in the limited range where ALE is observed for AlGaAs, it can be claimed that TMGa or TMAl molecules do not dissociate effectively on both the Ga and Al species forming the monolayer covered surface. This is based on the assumption that no dissociations of TMGa or TMA molecules take place in the gas phase.

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Figure 3 shows the dependence of the solid composition x and the 77K° PL emission energy on the gas phase composition of $Al_xGa_{1-x}As$ grown by ALE and MOCVD. The ALE films were grown at substrate temperatures of 550, 600 and 700°C, while the MOCVD films were grown at 800°C. The composition of the MOCVD films, as shown in Figure 3, depends on the $\frac{TMA}{TMA+TMGa}$ ratio and is consistent with previously reported results of AlGaAs growth by this technique. Figure 3 shows that Al incorporates during ALE more efficiently than in MOCVD.
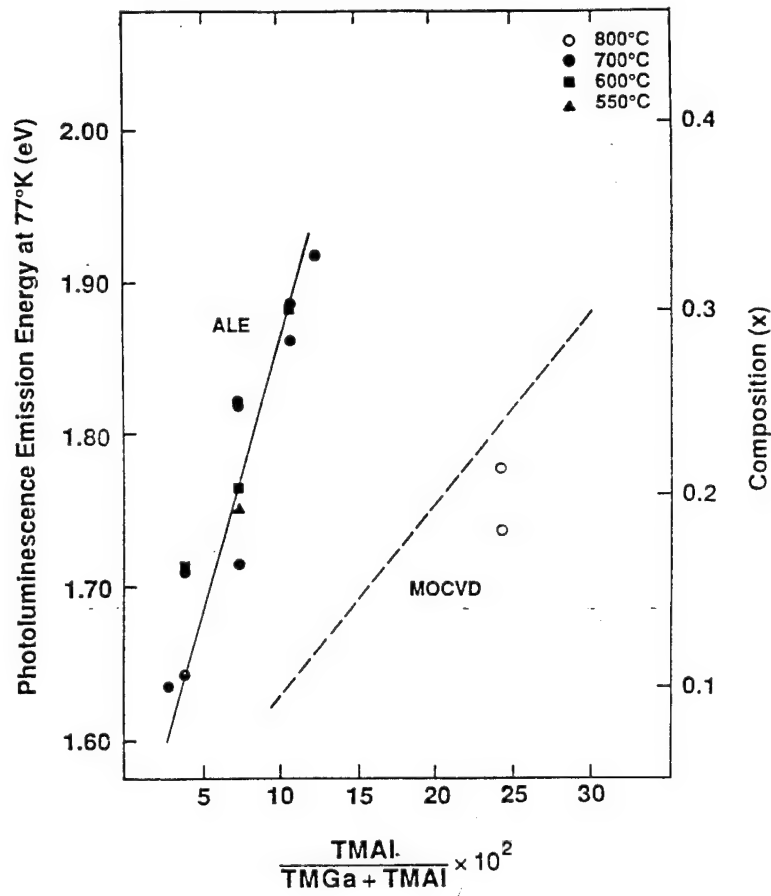
Figure 3 Photoluminescence emission energy at 77°K of $Al_xGa_{1-x}As$ and corresponding solid composition x as function of $\frac{TMA}{TMGa+TMA}$ molar ratio in column III stream.

Figure 4 shows the photoluminescence spectral for $Al_xGa_{1-x}As$ for different values of x grown by ALE and MOCVD. The MOCVD film grown at 700°C showed very weak emission, as shown in Figure 4(a). There were no PL signals observed from MOCVD films

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grown below 700°C. However, ALE grown films showed fairly strong PL peaks for growth temperatures as low as 600°C and a weaker emission at 550°C, as shown in Figure 4(b) and 4(c), respectively. This is considered to be one of the lowest temperatures where AlGaAs was grown with good optical properties. It should also be mentioned that 0.5 μm ALE films with indirect AlGaAs buffer layers grown at 600 and 700°C have a comparable PL intensity to 4 μm MOCVD films grown at 800°C. The ALE process allows an improvement in the PL properties that can be related to an enhancement in the surface migration of column III adsorbed atoms. It has been shown that Al and Ga species have high surface diffusion coefficient in the absence of AsH_3 or As_2 exposure.[10] This may result in improving the quality of ALE films, but it would not explain a difference in the incorporation mechanism of oxygen in the two techniques which may be responsible for the PL results. It may be possible that TMA is the source of oxygen, and a lower TMA flux in the ALE growth is accompanied by reduced oxygen incorporation in the grown films.
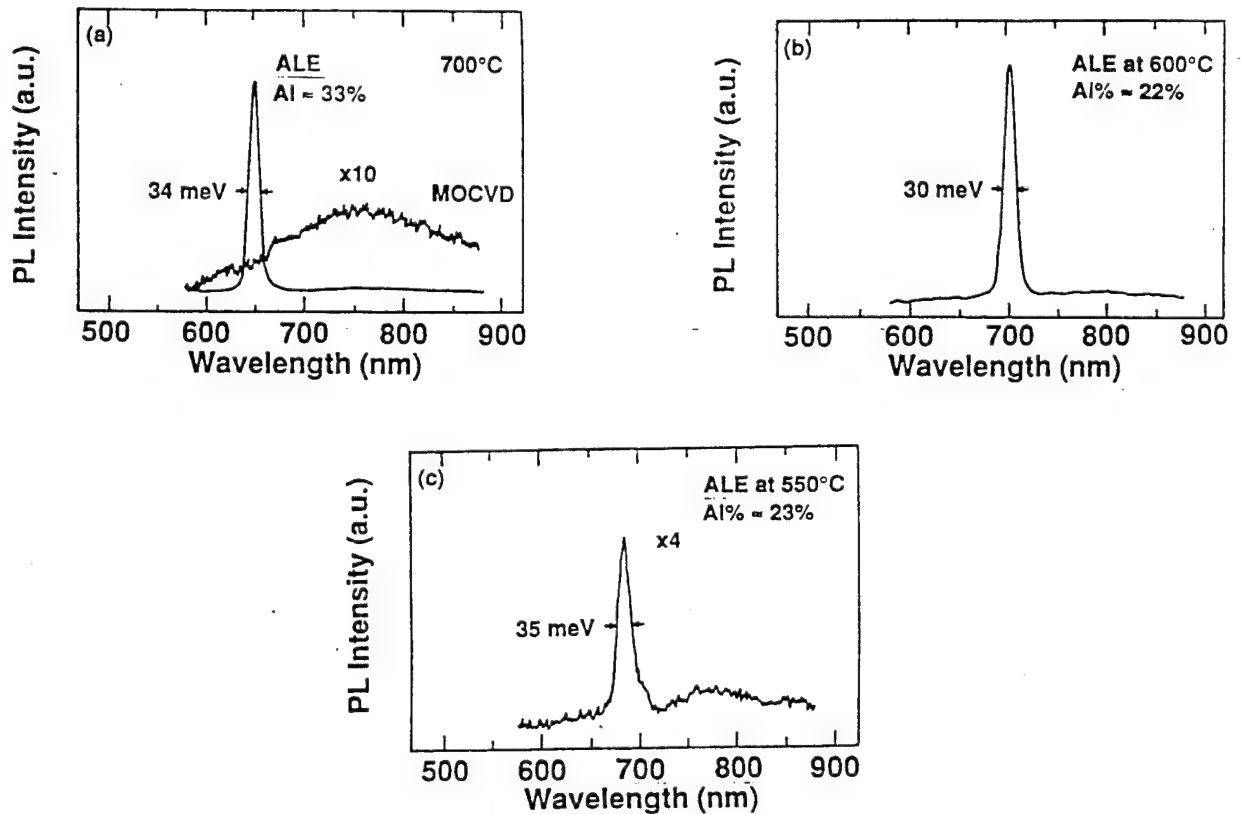

Figure 4 Photoluminescence at 77°K of AlGaAs grown by MOCVD and ALE at different temperatures a) ALE and MOCVD at 700°C, b) ALE at 600°C, and c) ALE at 550°C. No PL signals were observed from MOCVD films grown below 700°C.

The AlGaAs ALE films are p-type and have carrier concentration in the 10^{18}–10^{19}/cm^3 range for most of the films studied attributed to carbon incorporation in the grown films. This is one of the highest p-type doping levels reported in AlGaAs. However, when the growth conditions were optimized,[7] carrier concentrations fell to the mid 10^{17}/cm^3 range. Details of this study will be reported elsewhere.

3.2 InGaP[11,12]

InGaP was deposited directly on GaAs substrate (100), 2° off towards [110]. TMGa, TEI (Triethylinduim) and phosphine (10% in H$_2$) were used as source materials. During growth, PH$_3$ flowed continuously on the column V side. While the substrate was under the PH$_3$ flow, TMGa was turned on and allowed to stabilize, then the substrate was rotated one revolution through the TMGa flux back to the PH$_3$ to deposit approximately a mono-layer of GaP. TMGa was then turned off and TEI was turned on and stabilized while traces of TMGa were purged out. The substrate was rotated through the TEI flux back to PH$_3$ to deposit approximately a monolayer of InP, and thus a Ga-P-In-P structure was deposited. The structure was deposited at substrate temperatures in the range 480-600°C. The grown layers were characterized by X-ray diffraction, photoluminescence, photoreflectance, and transmission electron microscope techniques.

GaInP grown films at 500 and 550°C showed high-quality, smooth surface morphology when examined by Nomarski interference contrast microscopy.[11] Samples grown at 600°C showed increasing opacity. This may be due to the rapid surface depletion of P while the substrate is not PH$_3$ stabilized during the ALE rotation cycle. Double crystal X-ray diffraction rocking curves shown in Figure (5) have the (311) peaks of the GaAs substrate and InGaP epilayer. The relatively broad peaks for the substrate and the InGaP film are due to the limitations of our experimental X-ray set up. The ternary $Ga_{1-x}In_xP$ alloy grown at 500°C (sample A) has a peak corresponding to x $\approx$ .43 with mismatch to the sub-strate of about 0.3% [Figure 5(a)]. The sample grown at 550°C has x $\approx$ 0.49 and a mismatch of about < 0.1% as shown in Figure 5(b). It should be mentioned that the TEI and TMGa fluxes for these epitaxial films were chosen arbitrarily.
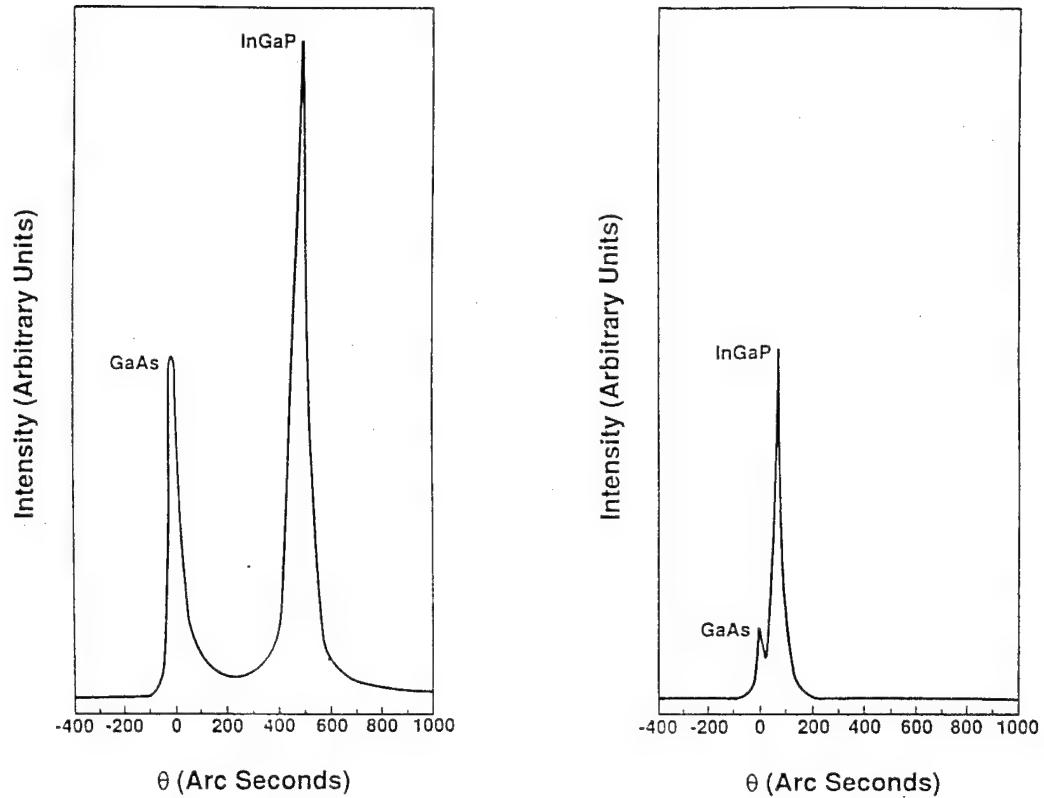
Figure 5 Double-crystal X-ray diffraction rocking curve for InGaP grown on GaAs substrate by ALE a) grown at 500°C, sample A, b) grown at 550°C, sample B.

The direct gap E_o was investigated using room-temperature photoreflectance. The experimental results are shown by the solid line in Figure 6. The dashed line is a least-squares fit to the Aspenes third-derivative functional form for a three-dimensional critical point.[13] For InGaP sample A we find an energy gap of 1.797 ±0.010 eV, as denoted by the arrow at the bottom of the figure, and a broadening parameter of 0.093 eV. Other samples grown using the same ALE growth sequence, the same TEI and TMGa fluxes while doubling the PH_3 flux, have E_0 of 1.778 eV. To the best of our knowledge, these band-gap values are the lowest reported for this compound and are close to the theoretical prediction reported by Zunger.[14] Photoluminescence (PL) at liquid Helium temperatures (~ 4 K) was also performed on sample A. The PL spectrum has a sharp peak at 1.868 eV with FWHM of about 30 meV.
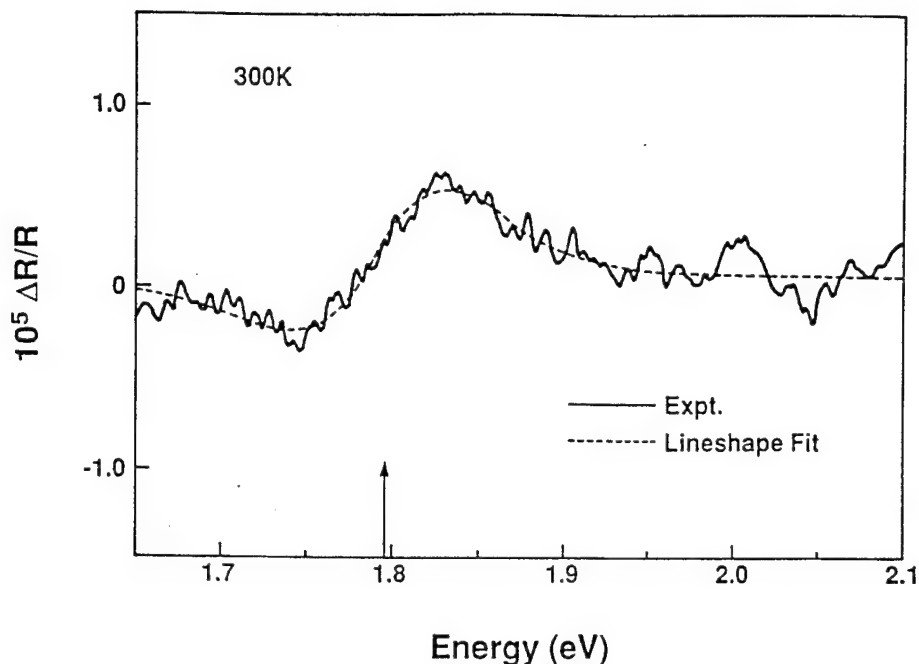
Figure 6 Photoreflectance spectrum at 300K (solid line) of InGaP sample A grown on a GaAs substrate. The dashed line is a least-squares fit to a third-derivative functional form for a three-dimensional critical point. The obtained value of the energy gap is indicated by the arrow at the bottom of the figure.

Cross-sectional transmission electron microscope (TEM) was also performed on these samples. Electron diffraction pattern for the [110] zone axis has extra superlattice spots which are distinct and well defined, indicating the CuPt type of ordering. Ideally, with the ALE deposition regime for this alloy, we would expect the column III sublattice to be ordered in the [001] growth direction. Although we found no evidence of a (001) superlattice from our diffraction studies, preferential ordering took place in (111) alternating planes. Detailed TEM studies of these ALE-grown films and the effect of growth conditions on the degree of ordering are under way.

1.4 SIDEWALL GROWTH BY ALE

Previously, deposition on GaAs grooves has been attempted both by conventional metalorganic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). They both show problems due to inherent growth mechanisms which are difficult to overcome. With MOCVD, gas hydrodynamics (mass transfer) causes film thickness variation inside grooves, leading to nonuniform growth and even no growth on specific surfaces.[15] Growth discontinuities have also been observed near the transition between superlattice structures grown on differently oriented adjacent planes. With MBE no growth occurs under the mesa overhang due to shadowing effects. Moreover, growth rates on differently oriented crystal planes vary because of the difference in the source beam impingement angles combined with sticking coefficient dependence on crystallographic orientation.

Two types of grooves were patterned on GaAs (100) substrates, $2°$ off toward $<110>$, by conventional photolithography and wet chemical etching techniques. Stripe openings, 8-20 μm wide and 300 μm apart were aligned on the photoresist either along the $[01\bar{1}]$ or $[011]$ directions. For the $[01\bar{1}]$ oriented stripes, a $1H_3PO_4/1H_2O_2/3H_2O$ etching solution was used, resulting in nearly V-shaped grooves. In case of $[011]$ oriented stripes, a $1NH_4OH/1H_2O_2/5H_2O$ etching solution was used, resulting in an inverted-trapezoid-shaped groove surrounded by overhanging reverse mesa structures. The etching was done at $16°C$, and the grooves were 4-5 μm deep. The crystallographic orientation of the sidewalls was identified by precise angle measurements on the scanning electron microscope (SEM) image of $\{110\}$ cleavage planes.

GaAs/$In_{0.2}Ga_{0.8}$As strained multilayered structures were grown on the patterned GaAs substrates by both ALE and conventional MOCVD in the same reactor. For ALE growth, the substrate temperature was either 480 or $520°C$ and each GaAs layer consisted of 360 growth cycles, while that for InGaAs was 40 cycles. For MOCVD growth the substrate temperature was $630°C$. The $In_{0.2}Ga_{0.8}$As layers served as markers to show the development of the growth front on variously oriented surfaces. Four or five periods of the multilayer structure were grown, giving a total thickness of the order of 1μm, depending on the growth scheme.

Figure 7 shows a schematic of a five-period structure grown on $[011]$ oriented grooves, obtained from a cross-sectional SEM photograph. The GaAs layers appear as dark lines with the InGaAs layers sandwiched in between. It is clear from Fig. 7 that the thickness of the deposited film at the bottom of this groove, a (100) plane, is uniform over the whole surface and equal to that deposited on the (100) surface on top of the mesa. Such results have not been achieved either by MBE or MOCVD due to shadowing and gas

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hydrodynamic effects, respectively. Previously reported MOCVD growth at the bottom of a similar mesa structure shows nonuniformity with thinner films at the corner and thicker films at the middle region.[16]

(a)

(b)
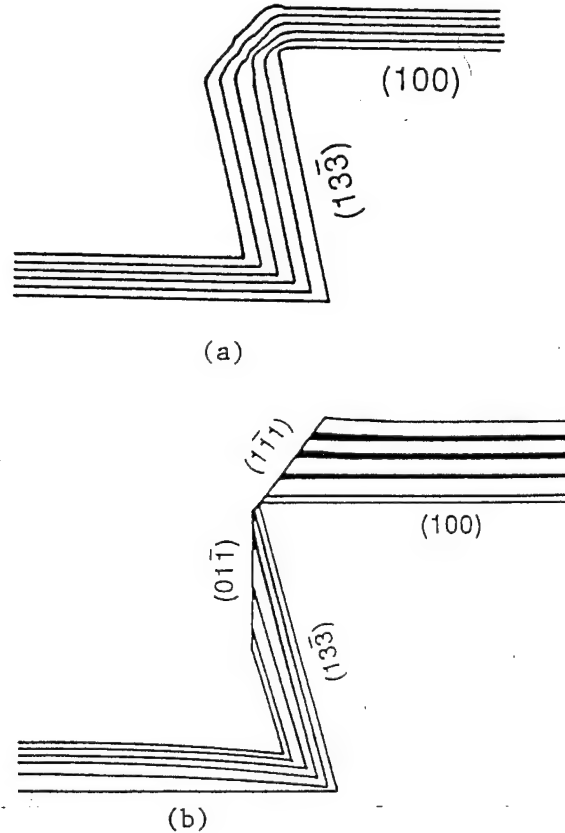
Figure 7 GaAs/InGaAs multilayer structure grown on a (100) GaAs substrate with [011] oriented grooves. (a) ALE (b) MOCVD

Growth on the (133) sidewalls is uniform over the entire surface with no apparent defects near the transition between the (133) and the (100) planes at the base of the groove. As was previously reported,[4] growth per cycle varies for differently oriented surfaces. For the sample shown in Fig. 7(a), the growth rate on the (100) surface is 1.3 monolayer (1.2x2.83 Å) per cycle while that on the (133) surfaces is approximately 2.16 Å per cycle. Samples grown under other growth conditions show different growth rates on the sidewalls. ALE growth on planes having mixed Ga and As atoms, such as (133), is not fully understood and in some cases the growth rate does not follow the predicted value.[19] Thus, we believe that more basic studies are needed.

Figure 7(b) shows a schematic made from an SEM photograph of a four-period multilayer structure grown on an identical groove using conventional MOCVD at 630°C. The growth on the (100) surface at the base of the groove is not uniform due to inherent mass transfer limitations, consistent with previous reports.[4,16] Also, the deposited film on the (100) original surface is thicker than that on the groove bottom. Growth on the sidewalls does not conform with the originally etched (133) planes, and thickness variations as well as formation of (01$\bar{1}$) facets are observed. Near the edge between the surface (100) plane and the etched (133) planes, growth is not continuous and (111)B facets are formed. This is probably due to the slow growth rate on (111)B surfaces often seen in MOCVD growth. The above results of conventional MOCVD growth are in striking contrast to ALE.

1.5 PLANAR DOPED STRUCTURES FOR NON-ALLOYED CONTACTS[17]

Atomic Layer Epitaxy (ALE) offers an attractive approach for the synthesis of δ-doped structures that can avoid some of the above mentioned problems. ALE is a low temperature growth process (400-500°C) which reduces dopant diffusion and prevents growth interruption by allowing only one temperature for the growth of an entire structure. With ALE, dopant atoms can be selectively introduced during either the Ga or the As exposure part of the ALE growth cycle, thus allowing the dopant to take the As or the Ga sites respectively. This can enhance dopant incorporation and reduce the compensation ratio. ALE also allows an accurate control of epilayer thickness between the dopant plane and the gate over a large area wafer, resulting in uniform values of pinch-off voltage and transconductance.

A growth rate of about 0.5 μm/h was used with the substrate in the temperature range of 450-500°C. The undoped ALE-grown GaAs is n-type with background carrier concentration in the low $10^{15}/cm^3$ range. This material is slightly compensated due to residual carbon contamination incorporated during the ALE process.

Carrier Concentration (cm⁻³) → 10^{20}, 10^{19}, 10^{18}
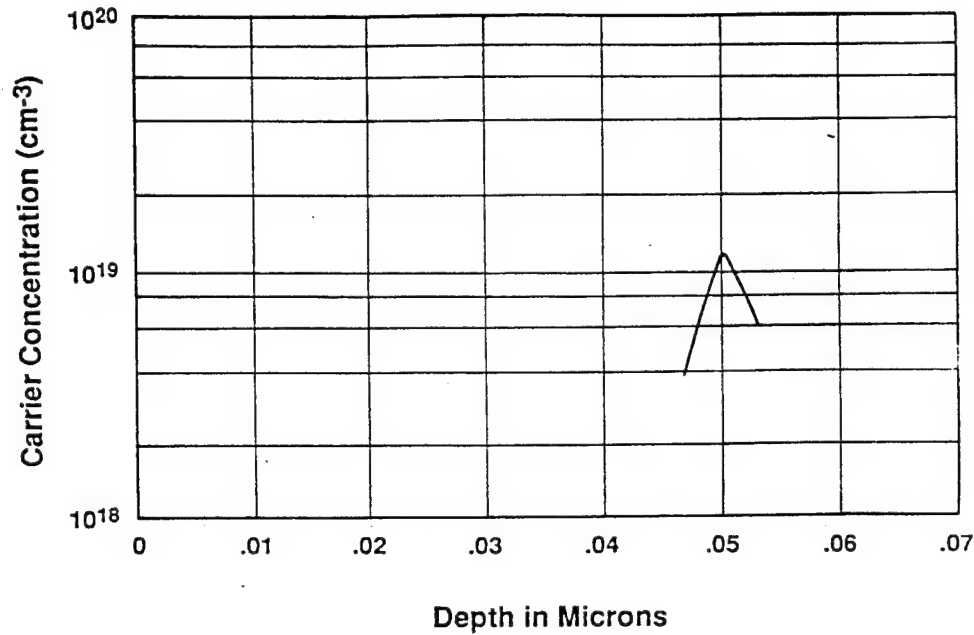
Depth in Microns → 0, .01, .02, .03, .04, .05, .06, .07

Figure 8 C-V profile of a delta-doped structure.

The δ-doped structure was grown by ALE on both Cr-doped and Si-doped GaAs substrates. H_2Se was introduced during the AsH_3 exposure part of the growth cycle with minimum AsH_3 flux (mass flow controller was set to its minimum value). This would allow the Se atoms to be efficiently incorporated in As sites. Exposure time to the H_2Se flux was on the order of 30 seconds and achieved carrier concentration that peaked in the $10^{18}/cm^3$ range as indicated from capacitance-voltage (C-V) measurements. Higher sheet carrier concentrations peaking in the $10^{19}/cm^3$ range was achieved by going through one or two ALE cycles with minimum AsH_3 and maximum H_2Se during the column V exposure. Figure 8 shows the C-V profile of a δ-doped structure grown on a Si-doped substrate. The structure is made of 1000 Å of undoped GaAs then a planar doped layer, followed by 500 Å of undoped GaAs all grown by ALE at the same temperature [500°C]. The observed C-V profile is sharp, peaking at about $10^{19}/cm^3$ with full width at half maximum (FWHM) of about 50 Å. The FWHM is comparable to the best reported planar doping achieved by MBE.[18] It should also be mentioned that previous efforts[19] to achieve planar doping by ALE using chloride sources had peak concentrations in the $10^{18}/cm^3$ range and FWHM of 80 Å.

This high carrier concentration achieved by planar doping can be used for nonalloyed ohmic contacts. In this work a set of ten Se planar-doped sheets, each separated by 50 Å of GaAs, was grown using ALE. Hall measurement for this structure gave carrier concentrations of $2 \times 10^{19}/cm^3$ for the 500Å epitaxial film grown on Cr-doped substrate. This value is considered one of the highest carrier concentrations reported for GaAs using metalorganic sources. It should be mentioned that the peak carrier concentration for these planar-doped sheets is higher than the above measured bulk value obtained from Hall measurement. The growth of this ALE structure was followed by metallization using Au-Ge-Ni. The nonalloyed contact has contact resistivity in the low $10^{-6} \, \Omega \, cm^2$, with a lowest measured value of $0.7 \times 10^{-6} \, \Omega \, cm^2$. The contact resistivity was measured using the transmission line method. We have not observed any improvement in the value of this contact resistivity upon annealing. These results show the potential application of ALE for nonalloyed contacts.

1.6 PLANAR DOPED FIELD EFFECT TRANSISTOR[17]

Figure 9 shows a schematic of the δ-doped FET grown by ALE at 500°C. It consists of a GaAs undoped buffer layer followed by five periods of GaInP/GaAs superlattice, a 500 Å undoped GaAs, a Se planar-doped layer peaking to about $10^{18}/cm^3$, then another 500 Å of undoped GaAs. The sample was then removed from the ALE reactor. Regions under the source and drain were chemically etched, followed by regrowth of n^+ contacting layers. The n^+ contacting layers are made of five planar doped sheets separated by 50 Å of GaAs and they thus allow direct contact to the planar doped sheet in the channel of FET. This approach was found to reduce the source and drain parasitic resistances and improve device performance. The dc characteristics of the δ-doped FET are shown in Figure 10. The FET has an extrinsic transconductance of 120 mS/mm and current density of 300 mA/mm for gate length and width of 1.2 and 300 μm, respectively. The gate source breakdown voltage was 8V. Finite output conductance and pinch-off difficulty are believed to be a result of the relatively high carrier concentration of the ALE-grown GaAs buffer ($1 \times 10^{16}/cm^3$), the Se memory effects, and the very small conduction-band discontinuity between the ALE-grown GaInP and GaAs.
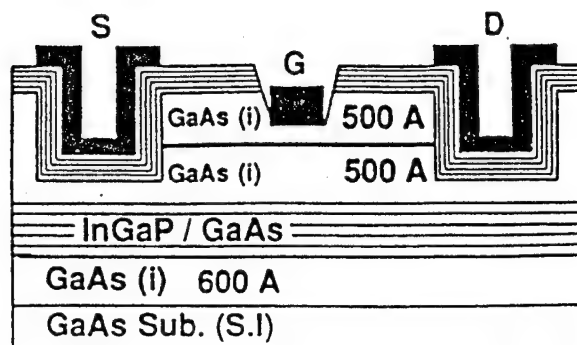
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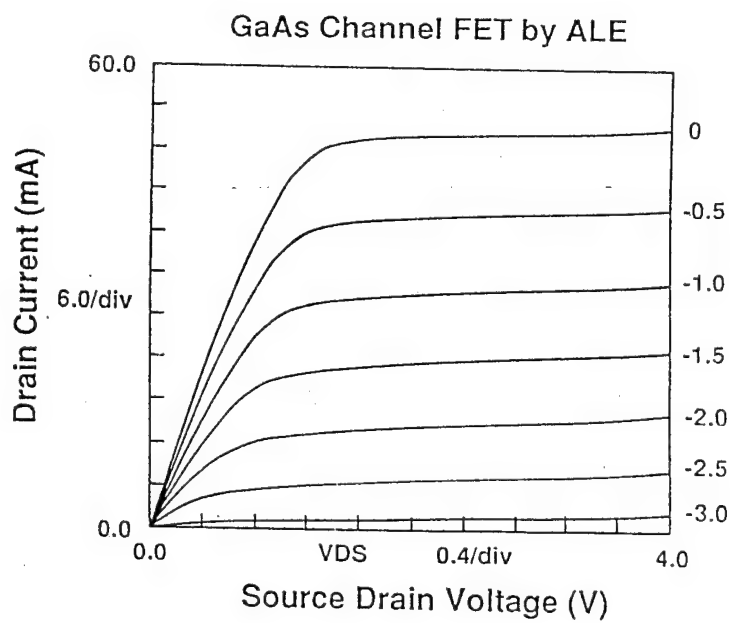Figure 9 Cross-section of delta-doped FET by ALE.

Figure 10 Drain current characteristics of delta-doped FET.

2   Advanced Devices and Circuits (Texas Instruments)

Atomic-layer epitaxy (ALE) has several unique capabilities relative to molecular-beam epitaxy (MBE) or metal-organic (MO) MBE that are desirable for advanced electron devices. These capabilities include monolayer thickness control in the growth direction, lateral uniformity across the wafer, abrupt and flat heterojunction interfaces to within a single monolayer, conformal overgrowth, and ordering of alloy semiconductors. This work has examined three device types that use some of these ALE advantages: the pnp heterojunction bipolar transistor (HBT), the delta-doped metal-semiconductor field-effect transistor (MESFET), and resonant tunneling devices.

In this work, we demonstrated, for the first time by ALE, the carbon-doped pnp HBT, delta-doped MESFETs with high transconductance, and the AlGaAs/GaAs resonant tunneling diode (RTD). In addition, we achieved conformal overgrowth of AlGaAs on etched GaAs structures, and the formation of high-quality quantum-well interfaces (as determined by photoluminescence) in the GaAs/AlGaAs and GaInP/GaAs systems.

2.1   *Heterojunction Bipolar Transistors*

The performance of high-speed and microwave HBTs depends strongly on the properties of the epitaxial layers that make up the device vertical structure, especially the base layer thickness and the position of the heterojunction relative to the electrical junction at the emitter/base interface. The precise control of these epitaxial layer properties by ALE is expected to significantly improve HBT performance. Since the performance of AlGaAs/GaAs pnp HBTs is inferior to their npn counterparts at present, and because ALE offers the ability to dope emitter and collector layers with carbon, we concentrated specifically on the pnp transistor.

ALE-grown GaAs/AlGaAs pnp HBTs were fabricated using our standard process for large-area mesa devices. A current gain of 120 with a collector-emitter breakdown voltage of 15 V and good common-emitter I-V characteristics were obtained. These HBTs are the first pnp HBT devices reported using carbon for the p-type dopant in the emitter and collector. Our results were published in *Electronics Letters*;[20] this paper is attached as Appendix I. The use of carbon, with its low diffusivity and the potential for doping up to 1×10^{20} in GaAs, is expected to lead to reduced emitter and collector resistances.

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2.2 Delta-Doped Field-Effect Transistors With Submicron Gate Length

Two different FET types were grown by ALE during this program. The first structure was a conventional MESFET and the second was a delta-doped MESFET. The MESFET structure consisted of an n+ contact layer followed by a 2.5×10^{17} cm^{-3} channel layer and an undoped buffer layer. The delta-doped structure had a similar layer structure except the active channel was replaced with an undoped layer with a planar sheet doping. Figure 2.1 is a cross section of the delta-doped MESFET. The advantages of the delta-doped structure over conventional MESFETs are higher sheet carrier concentration, higher breakdown voltage, and formation of a two-dimensional gas layer.
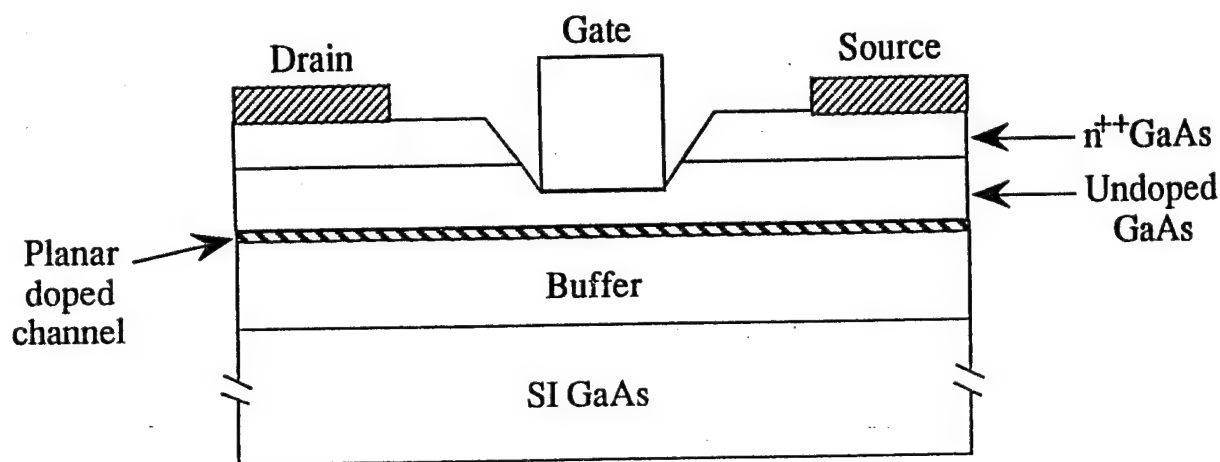

Figure 2.1. Delta-doped MESFET.

The material layer structures were first characterized by electrochemical C-V measurements to determine the doping profile. The wafers were then processed with Texas Instruments standard discrete FET process. The devices were 75 μm in gate width and 0.5 μm in gate length. Boron implantation isolated the devices. AuGeNi was used to form the device source and drain ohmic contacts. The gates (exposed by e-beam) were recessed below the n+ contact layer and into the active layer until a current value of approximately 250 mA/mm was achieved. TiPtAu was evaporated to form the gate contact. Bond pads and plated air bridges completed the devices. The devices contained coplanar lines for cascade on-wafer probing.

Table 2.1 lists the maximum transconductance, breakdown voltage, and cutoff frequency for the completed wafers with standard and delta-doped channels. The two MESFET wafers performed very well. A maximum transconductance (G_m) of 240 mS/mm was achieved with 12- to 13-volt breakdown voltage. The value of F_t was 22 to 27 GHz. These values are comparable to those obtained with the same structure grown by MBE.

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Table 2.1. ALE MESFET Performance

Wafer	Structure	G_m (mS/mm)	V_b (V)	F_t (GHz)
E-126	MESFET	240	13	27
E-145	MESFET	240	12	22
E-127	d-MESFET	347	1	
E-128	d-MESFET	320	2	21
E-146	d-MESFET	66	7	10
E-150	d-MESFET	400	1	
E-185	d-MESFET	320	1	
E-258A	d-MESFET	417	2	21
E-258W	d-MESFET	311	5	20
E-94	d-MESFET	227	10	
E-95	d-MESFET	227	16	
E-96	d-MESFET	227	15	

The results from the delta-doped MESFET were more variable and inconsistent; however, very good transconductance values comparable to HEMTs were obtained. There were two difficulties with the delta-doped MESFET. First, the devices did not pinch off very well, and second, the breakdown voltages were low. It is believed that this results from poor buffer layers and high background doping. Much of the work on the delta-doped structures was in optimizing growth of the undoped GaAs. The last three wafers were successful in improving the quality of the material as shown by the high breakdown voltages, which were was as high as 16 volts. The best overall results were obtained on wafer E-258A. The transconductance was as high as 417 mS/mm, which is comparable to a HEMT. Figures 2.2(a) through 2.2(c) show the dc and RF characteristics of this device. The value of F_t for this device was 21 GHz.

2.3   *Quantum Well/Resonant Tunneling Heterostructures*

Development of resonant tunneling devices and circuits requires critical dimensional control in both the lateral and vertical directions and the ability to form lateral heterojunctions. MBE, which has heretofore produced the materials for resonant tunneling transistors, diodes, and quantum dots, is limited in that it does not provide monolayer thickness control or conformal overgrowth on etched structures.
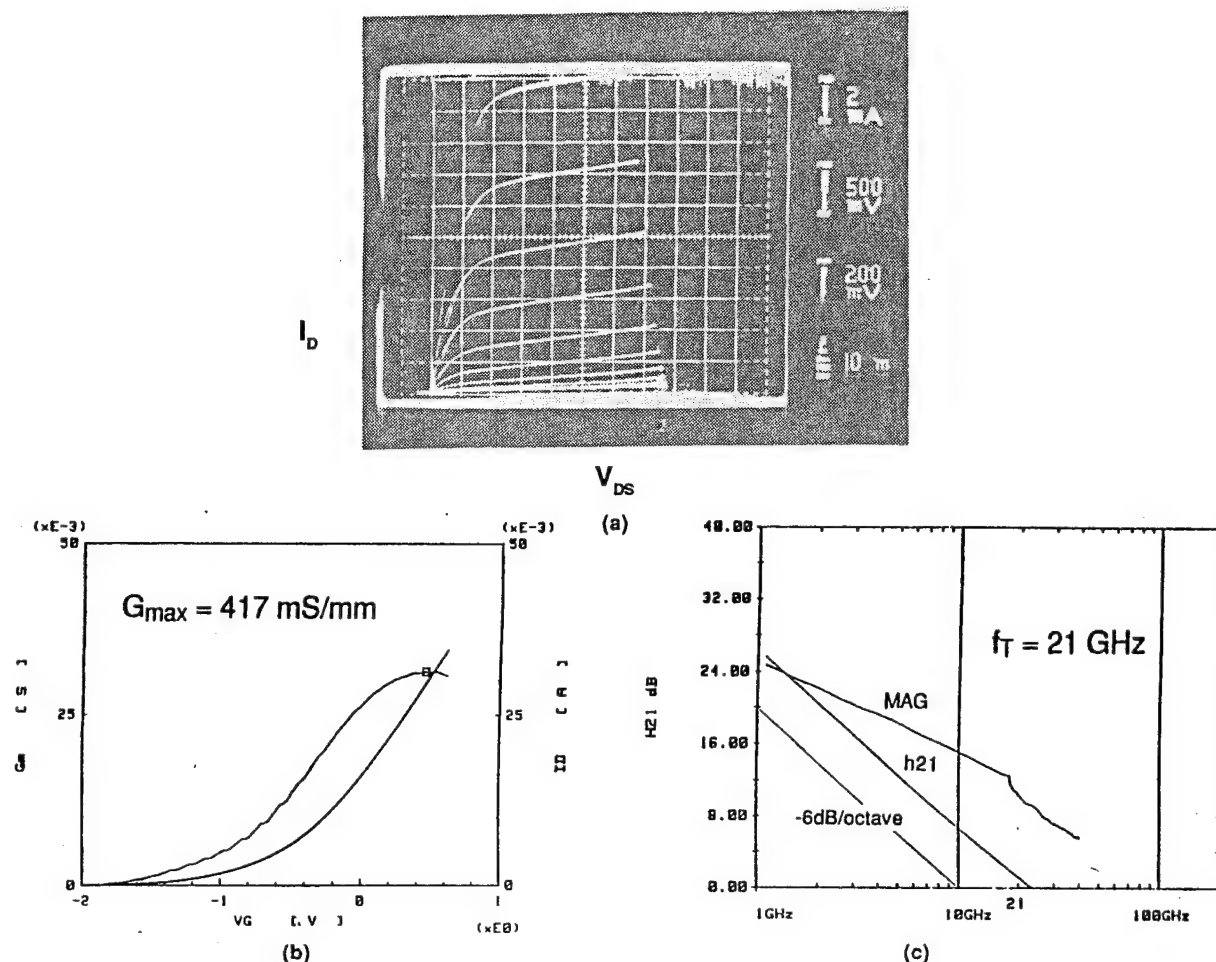
Figure 2.2. Delta-doped MESFET measured dc and RF performance: (a) I-V, (b) G_m versus V_{gs}, and (c) h_{21} versus frequency.
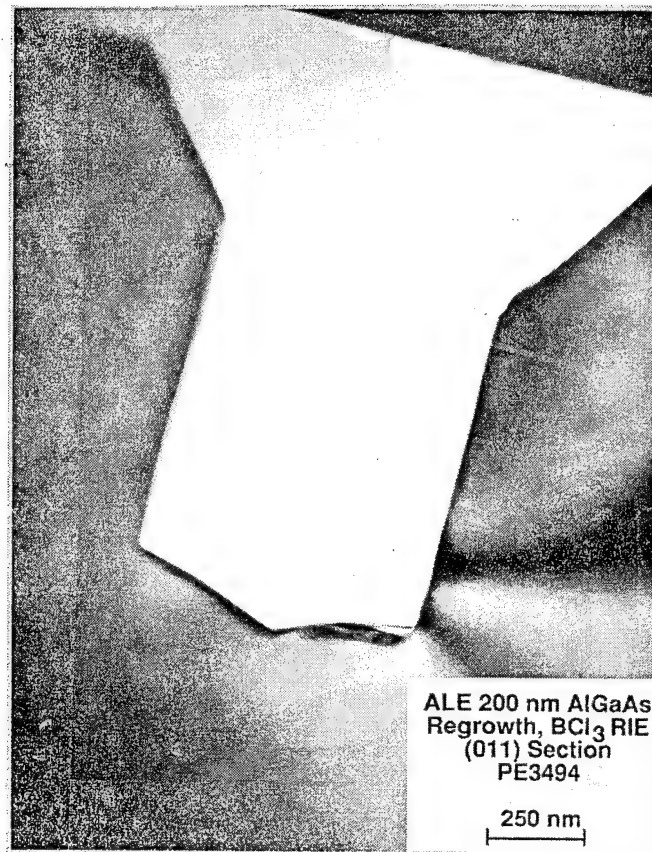
Conformal overgrowth of AlGaAs on GaAs etched structures is shown in Figures 2.3 and 2.4. In these structures, etched trenches were formed by reactive ion etching GaAs in BCl_3 at Texas Instruments. These structures were then shipped to North Carolina State University for epitaxial overgrowth and returned for evaluation. Figures 2.3 and 2.4 are transmission electron micrographs of the overgrowth of 200 nm of AlGaAs on 1-μm-deep etched trenches. The figures show two cross sections of the (011) plane cleaved perpendicular to one another. Where the interface is visible, an abrupt overgrowth, without dislocations and conformal to the sidewall, is observed. These results suggest that conformal overgrowth can be used to form lateral resonant tunneling devices. A mask set to use the overgrowth in lateral resonant tunneling diodes and transistors was designed and fabricated. Device development is under way.

A prerequisite to forming the lateral resonant tunneling device is demonstration of a vertical RTD grown by ALE. This was accomplished under this contract (and to our knowledge has not been previously demonstrated). The device layer diagram is as shown in Table 2.2. Thin (3-nm) tunnel barriers helped minimize the thickness of the AlGaAs layers, which are known to have high background carbon density.

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ALE 200 nm AlGaAs
Regrowth, BCl$_3$ RIE
(011) Section
PE3494

250 nm
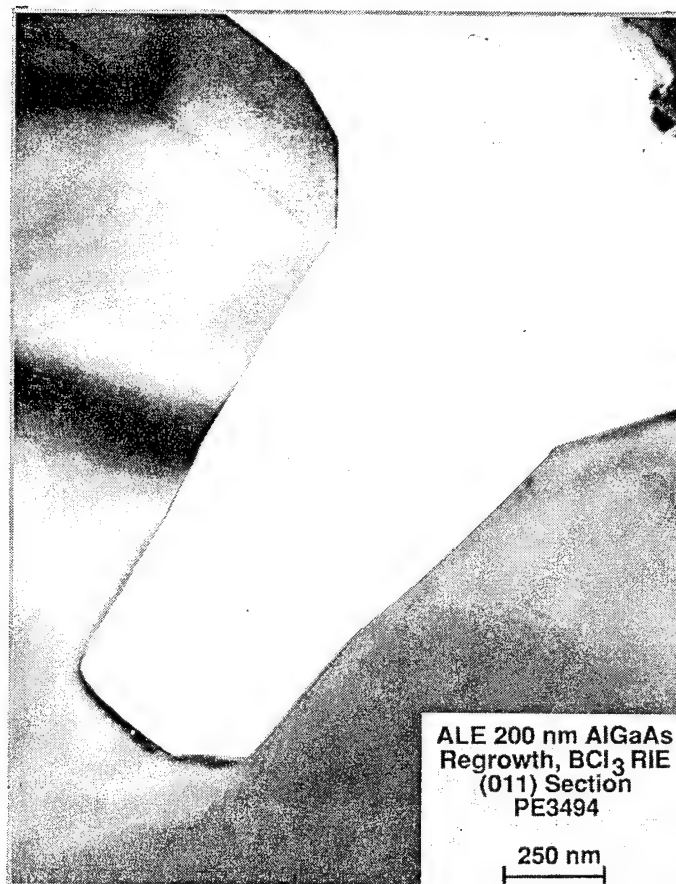
Figure 2.3. Conformal overgrowth of 200 nm of AlGaAs on an etched GaAs trench.

ALE 200 nm AlGaAs
Regrowth, BCl$_3$ RIE
(011) Section
PE3494

250 nm

04751

Figure 2.4. Conformal overgrowth of 200 nm of AlGaAs on an etched GaAs trench; this (011) plane is perpendicular to that shown in Figure 2.3.

300 nm	GaAs	6 to 9 $\times 10^{17}$ cm^{-3}
30 nm	GaAs	–
3 nm	$Al_{0.3} Ga_{0.7} As$	–
5 nm	GaAs	–
3 nm	$Al_{0.3} Ga_{0.7} As$	–
30 nm	GaAs	–
300 nm	GaAs	6 to 9 $\times 10^{17}$ cm^{-3}
n$^+$ GaAs substrate		

The current-voltage (I-V) characteristics of this device at room temperature and 77 K are shown in Figure 2.5. Clear negative differential resistances (NDRs) are observed at 77 K at a voltage of greater than 1 V for both bias polarities. To understand this I-V characteristic, we have computed the potential profile of the device and solved for the quasibound states.[21] In Figure 2.6(a), the band diagram for this double barrier is shown for the case in which the background doping in the undoped layers is 1×10^{15} cm^{-3}, n-type. The quantum-well ground state is approximately 145 meV above the conduction-band minimum; therefore, the resonant peak voltage is expected to occur at approximately twice this value, or 290 meV. Figure 2.6(b) shows the case in which the undoped layers have a concentration of 1.5×10^{17} cm^{-3}, p-type. Ionized carbon acceptors increase the potential height of the double barrier relative to the neutral n-type regions of the device.
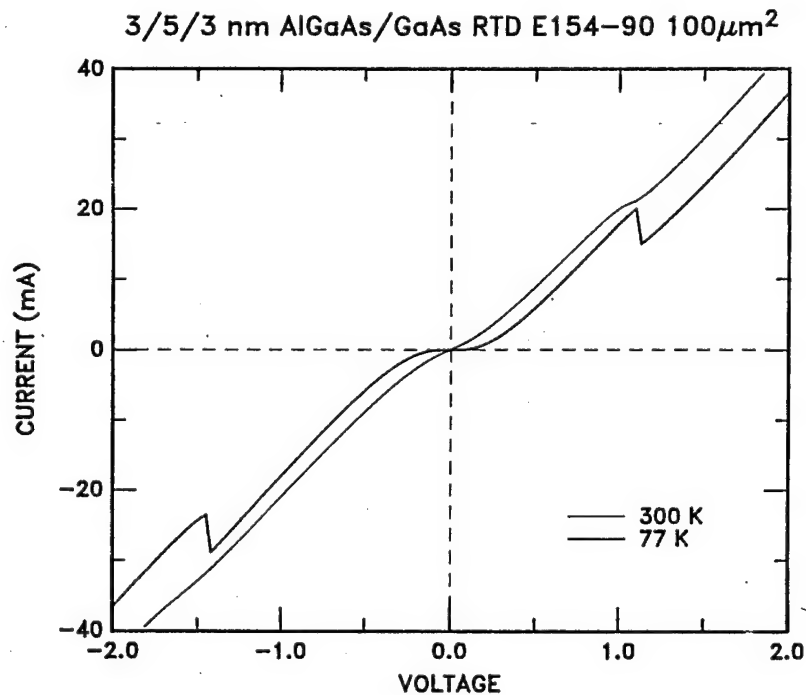
Figure 2.5. Current-voltage characteristics of an AlGaAs/GaAs resonant tunneling diode grown by ALE (wafer E-154-90).
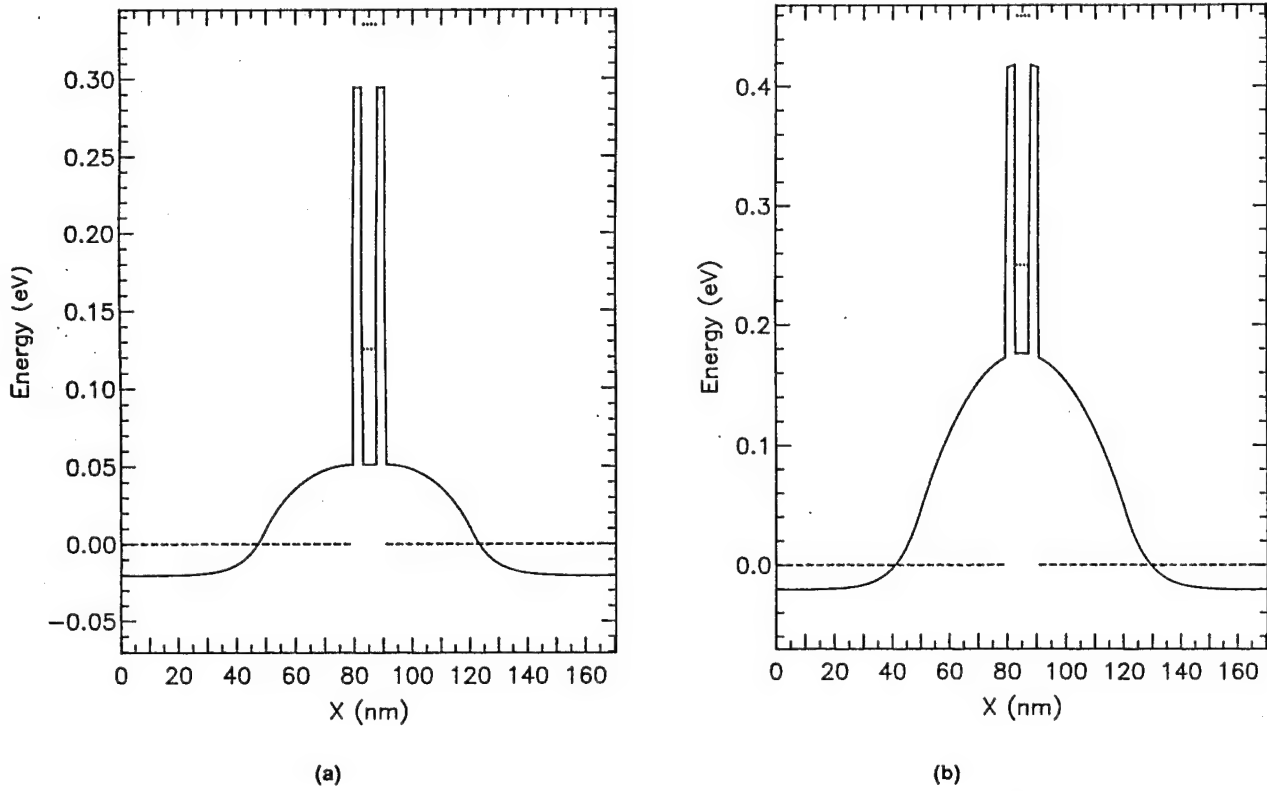
Figure 2.6. Computed energy-band diagram for the 3/5/3-nm $Al_{0.3}Ga_{0.7}As$/GaAs RTD with 30-nm spacer layers, contact doping of 6×10^{17} cm^{-3}, and (a) undoped background donor density of 1×10^{15} cm^{-3} or (b) undoped background acceptor density of 1.5×10^{17} cm^{-3}.

For acceptor densities this high, the usual rule of thumb to estimate the RTD resonant peak voltage does not hold, because of the large voltage drop occurring across the p-regions. Figure 2.7 shows the calculation of the potential profile for the case of the p-type background acceptor density at near the resonant bias, 1 volt. Our observations of resonant tunneling at biases beyond 1 volt are consistent with an average p-type acceptor density of slightly greater than 1.5×10^{17} cm^{-3}.

We also compare the ALE RTD with a conventional MBE-grown AlGaAs/GaAs RTD with the same well width and barrier height (Figure 2.8). The layer structure for the MBE-grown device differs in other ways: the barriers are 5 nm wide, the undoped spacers are 5 nm, and the contact doping is 2×10^{18} cm^{-3}, but the peak voltage should be the same. The MBE-grown device goes into resonance at approximately 300 meV as expected. Comparison of the current densities for the two devices, however, shows a factor of more than 300 difference in current density for the two devices. This is consistent with the formation of a potential hill on the injector side of the RTD at high biases, which limits the current flow into the device (Figure 2.8).
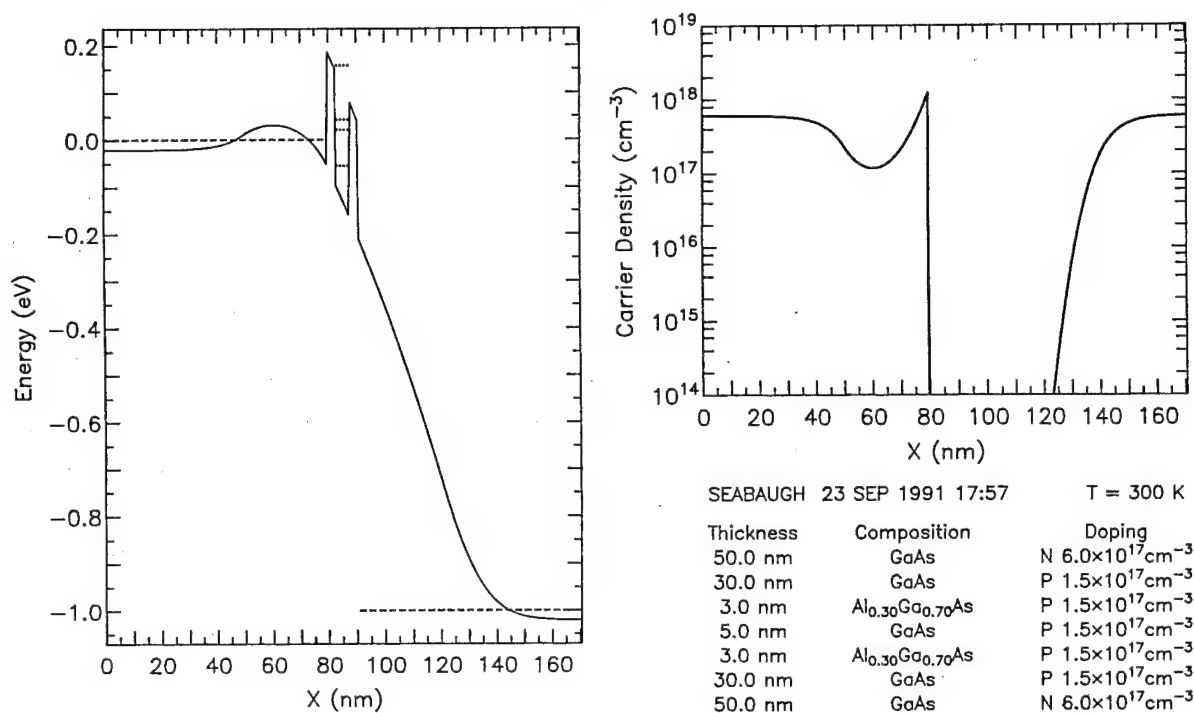
23

Energy (eV)

0.2

0.0

−0.2

−0.4

−0.6

−0.8

−1.0

0   20   40   60   80 100 120 140 160

X (nm)

Carrier Density (cm^{-3})

10^{19}

10^{18}

10^{17}

10^{16}

10^{15}

10^{14}

0   20   40   60   80 100 120 140 160

X (nm)

SEABAUGH   23 SEP 1991 17:57   T = 300 K

Thickness	Composition	Doping
50.0 nm	GaAs	N 6.0×10^{17}cm^{-3}
30.0 nm	GaAs	P 1.5×10^{17}cm^{-3}
3.0 nm	Al$_{0.30}$Ga$_{0.70}$As	P 1.5×10^{17}cm^{-3}
5.0 nm	GaAs	P 1.5×10^{17}cm^{-3}
3.0 nm	Al$_{0.30}$Ga$_{0.70}$As	P 1.5×10^{17}cm^{-3}
30.0 nm	GaAs	P 1.5×10^{17}cm^{-3}
50.0 nm	GaAs	N 6.0×10^{17}cm^{-3}

Figure 2.7. Computed energy-band diagram and carrier-density profile for the RTD of Figure 2.6(b) under 1-volt bias.

5/5/5 nm AlGaAs/GaAs RTD Comparison 77 K

CURRENT DENSITY (A/cm^2),

1.5×10^4

1.0×10^4

5.0×10^3

0.0×10^0

−5.0×10^3

−1.0×10^4

−1.5×10^4

−1.0   −0.5   0.0   0.5   1.0

VOLTAGE

CURRENT DENSITY (A/cm^2)

5.0×10^2

2.5×10^2

0.0×10^0
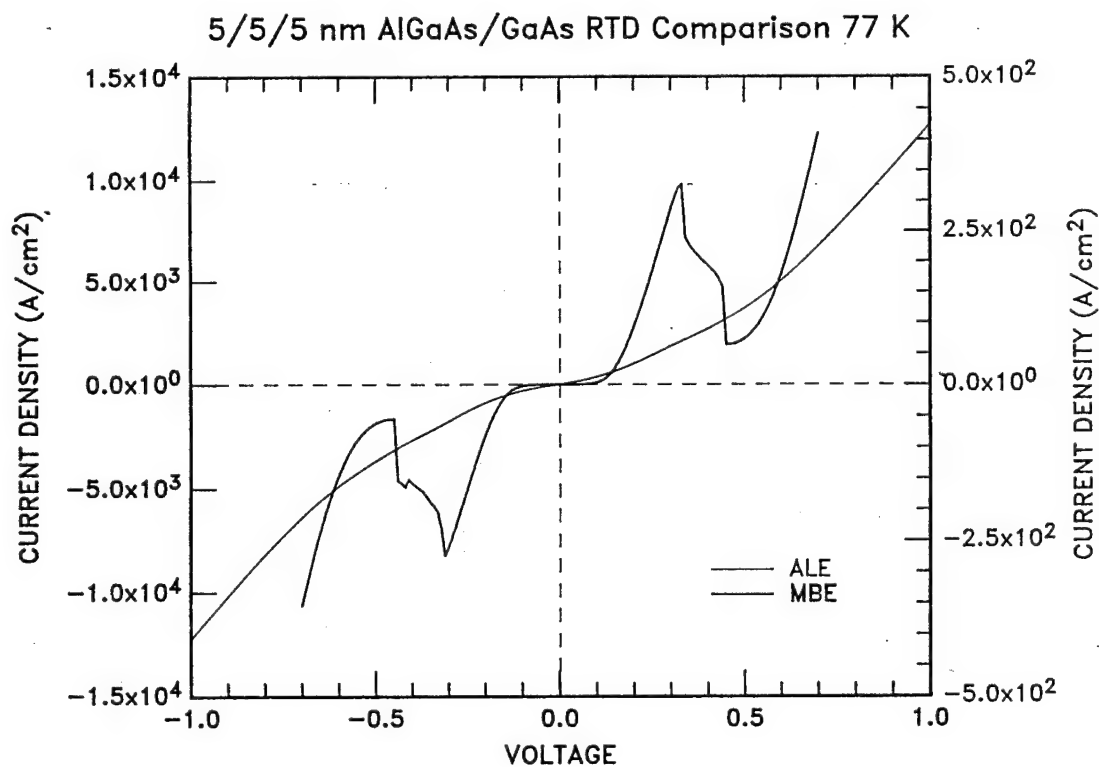
−2.5×10^2

−5.0×10^2

—— ALE
—— MBE

Figure 2.8. Comparison of the current-density versus voltage characteristics of the AlGaAs/GaAs ALE RTD (wafer E-154-90) with a comparable MBE-grown RTD (wafer R1322).

A second RTD was also demonstrated under this contract. This RTD was grown in the Emcore ALE reactor in a configuration in which the molybdenum baffles were removed (to eliminate a silicon-doping memory effect). These baffles are used to suppress mixing of the column III and V elements; therefore, in this mode, some gas mixing is possible. The RTD layer diagram is presented in Table 2.3.

Table 2.3. Layer Diagram of ALE-Grown Resonant Tunneling Diode, Wafer E-74-91C

320 nm	GaAs	1×10^{18} cm^{-3}
26 nm	GaAs	–
4 nm	AlGaAs	–
5 nm	GaAs	–
4 nm	Al GaAs	–
26 nm	GaAs	–
320 nm	GaAs	1×10^{18} cm^{-3}
n$^+$ GaAs substrate		

Room-temperature resonant tunneling in the ALE-grown RTD is observed for the first time in this device (Figure 2.9) with resonant peak voltage closer to the expected value of 300 meV. The low resonant peak voltage is an indication that the background carbon density is reduced in this growth mode and current density comparable to the MBE-grown AlGaAs/GaAs RTD is obtained.
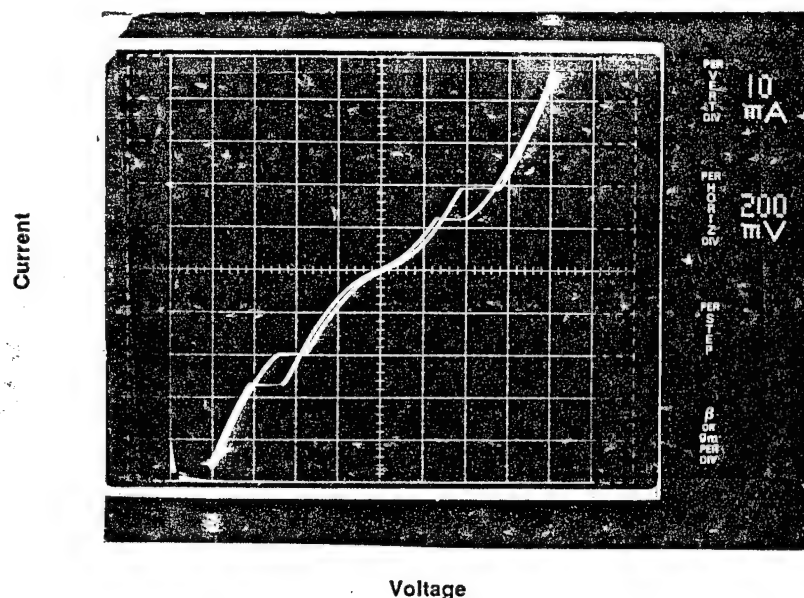
Figure 2.9. Room-temperature current-voltage characteristics of an AlGaAs/GaAs ALE-grown resonant tunneling diode (wafer E74-91C).

Monolayer thickness control is needed to ensure threshold voltage uniformity in logic circuit applications of the resonant tunneling diode. On this wafer (E-74-91C), we have mapped the uniformity of the peak current density and resonant peak voltage across the wafer. These results are shown in Figure 2.10. We find that the peak current density and peak voltage increase significantly near the leading edge of the rotating wafer. The higher currents are a result of thinner tunnel barriers, while the higher voltages correspond to thinner quantum wells. Thus, it appears that the growth rate is not saturating on the leading edge. Over the better part of the trailing edge, however, the voltage uniformity is within 10% and the current density, which is more sensitive to monolayer fluctuations, is 37%. These values are comparable to or slightly better than we achieve by MBE, and should improve with better isolation of the III and V sources.

2.4   Properties of ALE Films and Quantum Structures

During the course of this program, photoluminescence spectroscopy was used extensively to characterize the quality of films and quantum-well structures grown by ALE. Five binary or ternary alloy systems were studied: GaAs, GaInP (ordered and disordered), AlGaAs, GaP, and GaAsP. A total of 47 ALE samples were characterized, including both thick-film and quantum structures. Photoluminescence was performed using either a high-resolution dispersive spectrometer sensitive to photon energies between 2 and 1.46 eV or an interferometer-based spectrometer sensitive between 2 and 0.7 eV for the typical detector installations. Argon ion excitation at 514.5 nm was used in all cases. This section presents the results of measurements on the five semiconductor systems.

2.4.1   GaAs Films

Photoluminescence was used to identify residual impurity and defect characteristics in ALE GaAs layers. Figure 2.11 shows comparative PL exciton spectra at 1.6 K of ALE and MOMBE GaAs films. Note that the reference MOMBE sample is state-of-the-art for high-purity epitaxial GaAs. The ALE sample exhibits sharp excitonic features, indicating the specimen is high purity ($<1 \times 10^{15}$ atoms/cm^3) and high mobility. The exciton bands are labeled according to the assignments discussed by Williams and Bebb.[22] Evident in the ALE spectra is an additional defect-bound exciton feature (labeled G). In the case of MBE GaAs, the presence of G series defects is associated with low V/III ratios.[23] Although V/III ratio does not take its conventional meaning in the case of ALE GaAs, the presence of these defect centers is probably indicative of insufficient arsenic concentration during film growth. Interestingly, excitons bound to carbon acceptors are not evident in the spectrum of the ALE sample. The lack of carbon acceptor features in PL demonstrates that very low carbon concentrations can be obtained in ALE films prepared under some conditions. We previously reported the influence of V/III ratio on carbon incorporation and PL exciton spectrum.[5]

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**ALE AlGaAs/GaAs RTD
Wafer Maps**

leading
edge

E74-91C, 4/5/4 nm, 300K, 100 μm^2
Vp = 332 ± 33 (10%) mV, Ip = 11.25 ± 4.2 (37%)
PVR = 1.3 ± 0.2, injection toward surface.
Average and range taken over the flat
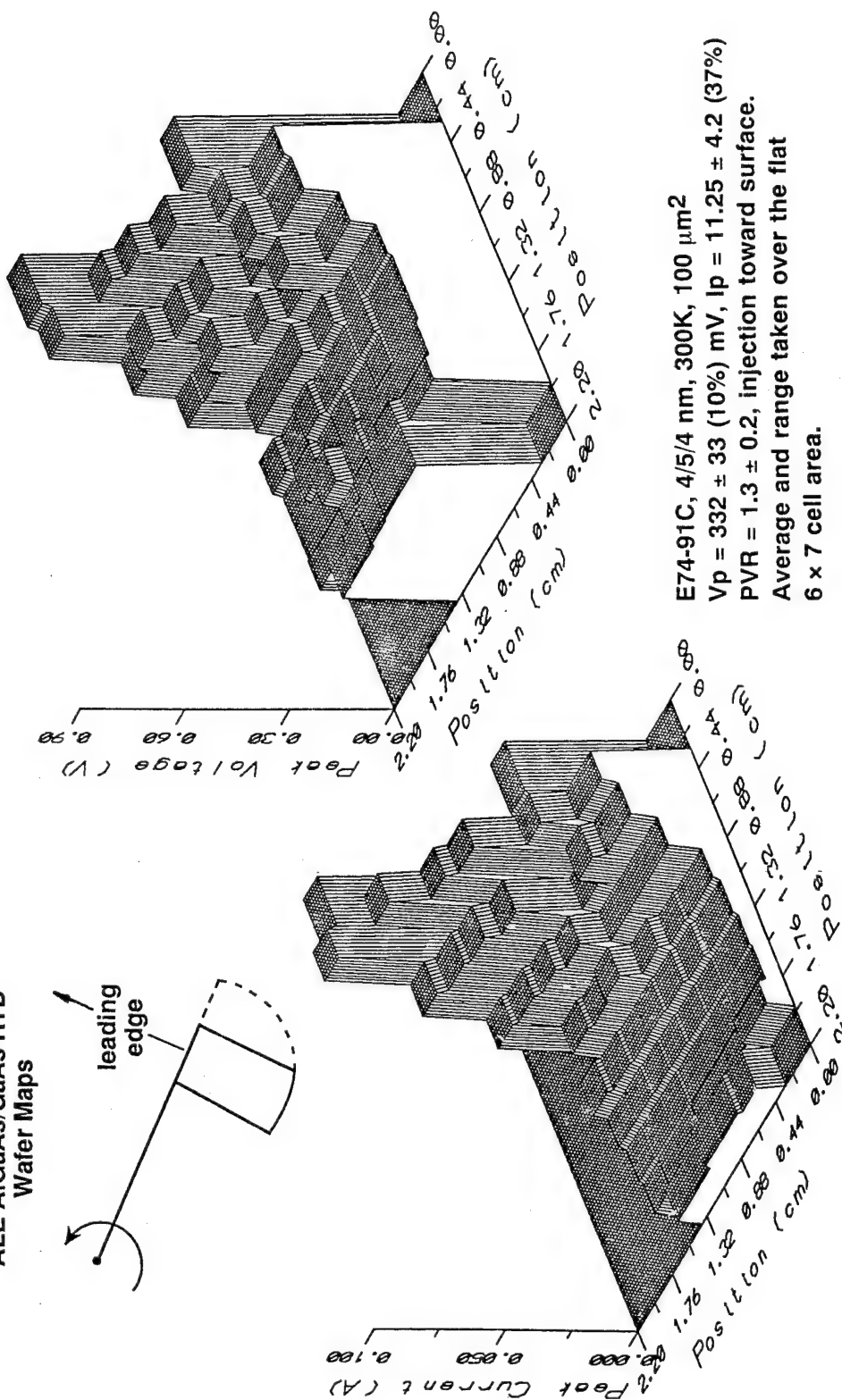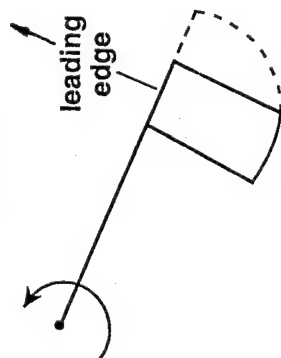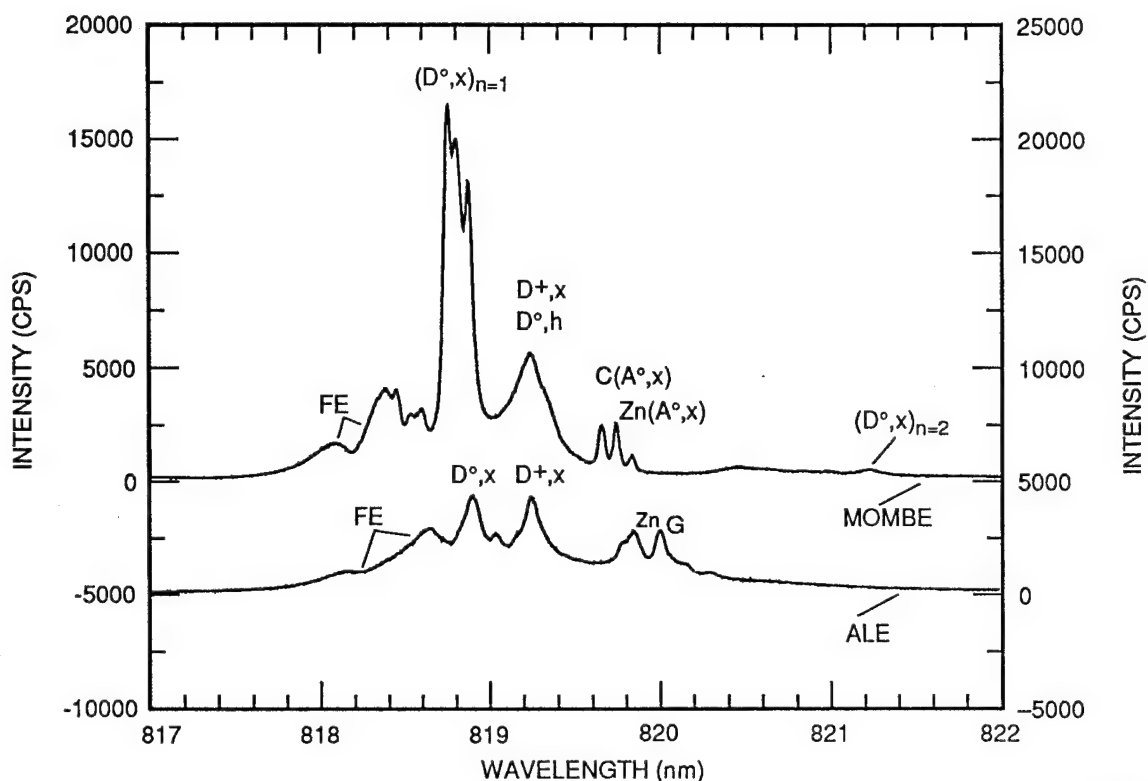6 × 7 cell area.

Figure 2.10.   Wafer maps of the RTD peak current density and resonant peak voltage for the ALE-grown
RTD (wafer E74-91C) at room temperature.

27

Figure 2.11. Low-temperature (1.6 K) photoluminescence spectra of high-purity ALE and MOMBE GaAs. The transitions observed are free exciton (FE), neutral donor-bound exciton (D°,X), ionized donor-bound exciton (D⁺,X), neutral carbon-acceptor bound exciton [C(A°,X)], neutral zinc acceptor-bound exciton [Zn(A°,X)], and defect-bound exciton (G).

Presented in Figure 2.12 is a representative liquid-helium temperature (4.2 K) PL spectrum of an ALE film recorded with spectral sensitivity to deep-level features to an energy of 0.7 eV. At high energy are the exciton and shallow impurity bands. The exciton region was discussed in detail previously. The ALE films studied have generally been free of any deep impurities or defects, as evidenced by the absence of bands below the shallow impurity features. Occasionally, deep-level features caused by copper at 1.355 eV or EL2 at 0.68 eV were observed. When observed, the copper probably resulted from the substrates and the EL2 from loss of stoichiometry control during film growth.
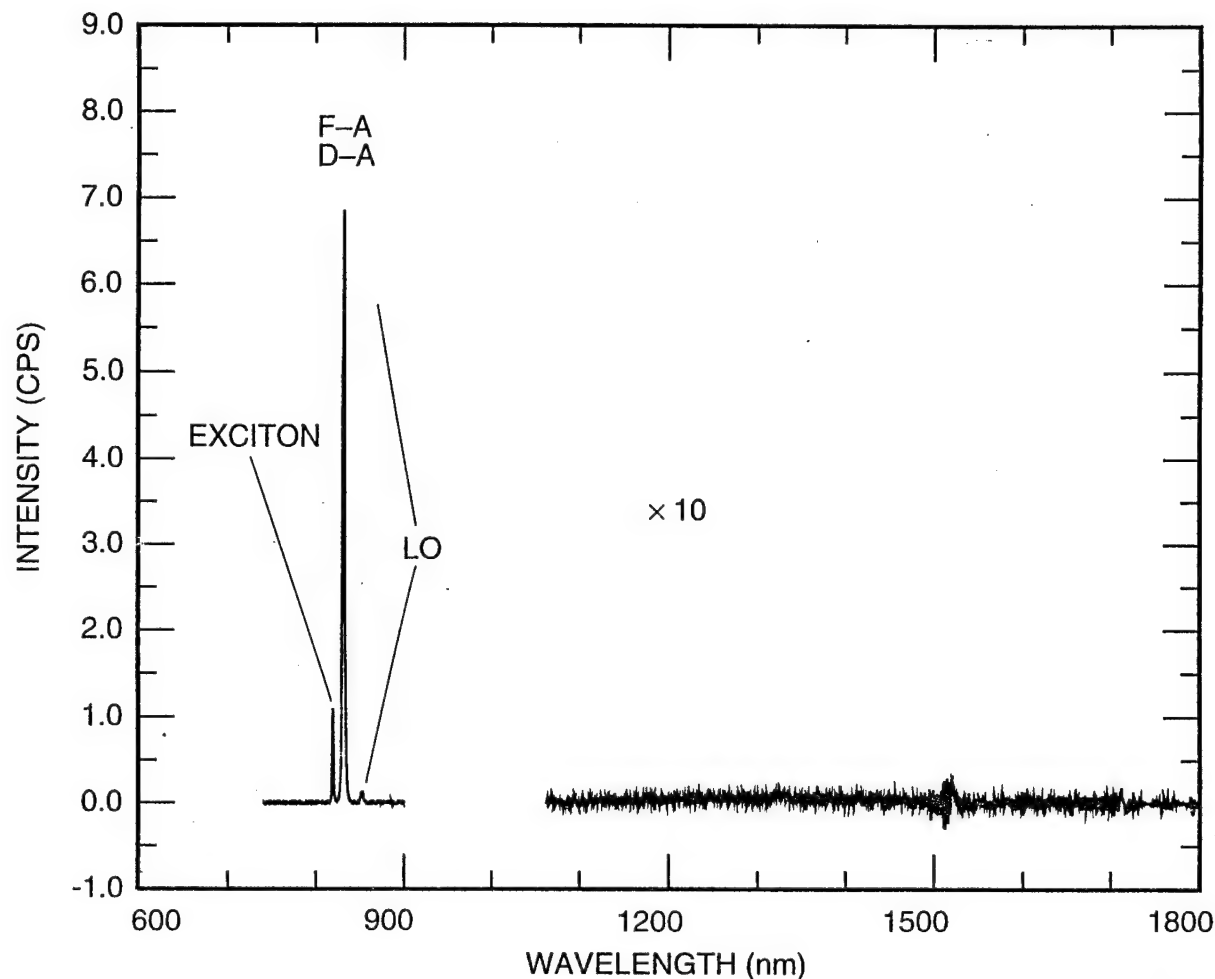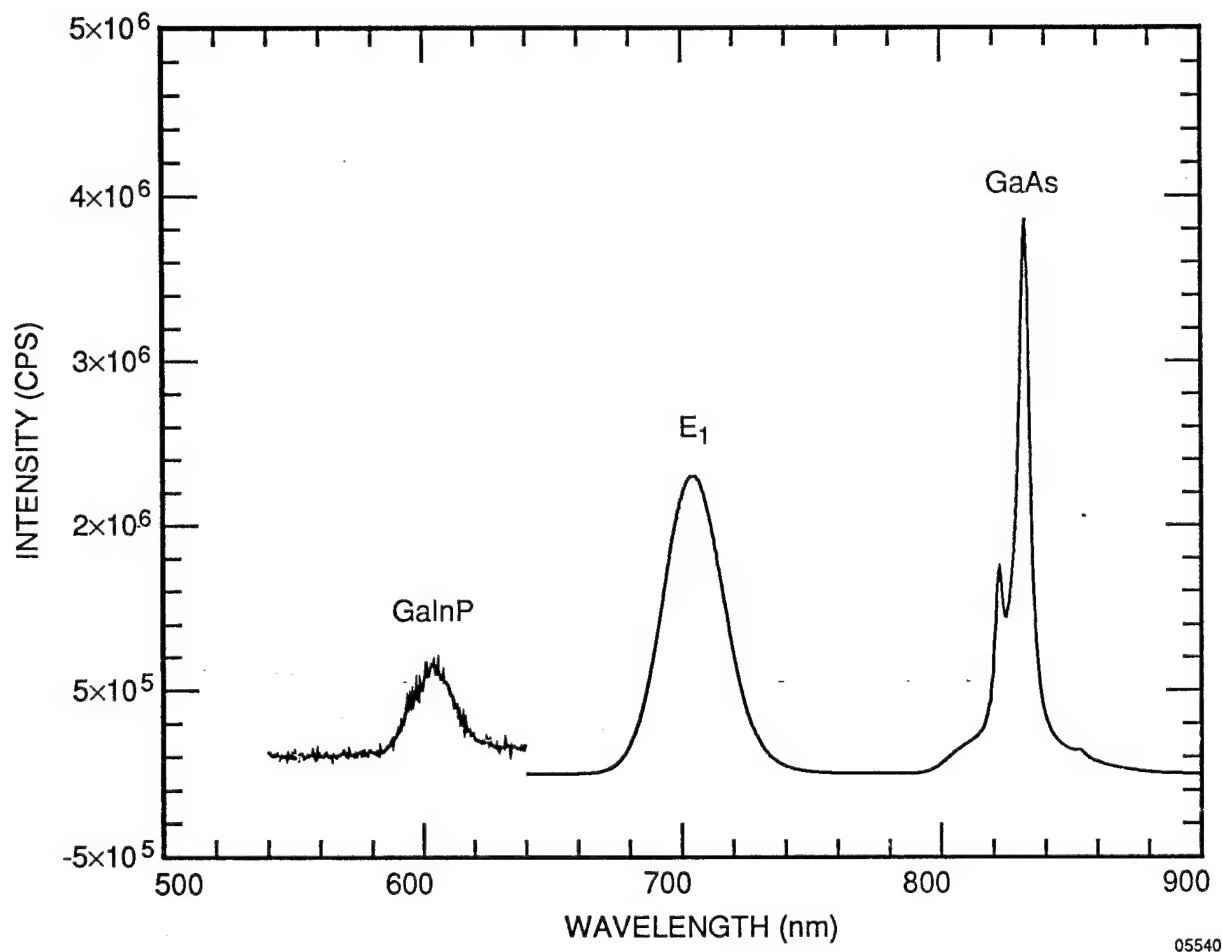
Figure 2.12. Low-temperature (4.2 K) photoluminescence spectrum of high-purity ALE with sensitivity to deep impurities and defects. Exciton, acceptor (F-A, D-A) and acceptor LO phonon replica (LO) are indicated.

2.4.2 GaInP Alloys

GaInP is an alternative wide-bandgap material to AlGaAs for forming barrier layers and other heterostructures with GaAs.[11] GaInP can occur as an ordered alloy, i.e., an atomic superlattice with alternating GaP/InP layers, or as a disordered alloy. Photoluminescence at liquid-helium temperature (4.2 K) of the ordered alloy yields a sharp peak at about 1.868 eV with a full-width half-height (FWHH) of typically about 30 meV. We previously reported the properties of the ordered alloy in Reference 5. GaInP/GaAs/GaInP quantum wells comprising either ordered or disordered GaInP were grown and studied. However, optical evidence of carrier confinement was observed only in quantum-well structures where the GaInP disordered alloy was used as barrier material. The reason why carrier confinement is not observed in wells with the ordered GaInP alloy barriers is not understood.

The photoluminescence spectrum of an GaInP/GaAs/GaInP quantum-well structure comprising disordered GaInP barrier layers is presented in Figure 2.13. Photoluminescence features originating from the barrier layers, the well, and the GaAs buffer layer are indicated in the spectrum. The behavior of PL line width versus well width for GaInP/GaAs/GaInP is presented in Figure 2.14. Although the theoretical behavior for PL line width versus well width is not available for this system, the observed PL line widths are appropriate for very narrow well widths. We believe these results on GaInP/GaAs quantum wells are unique and should be studied in more detail.

05540

Figure 2.13. Low-temperature (4.2 K) photoluminescence spectrum of ALE GaInP/GaAs/GaInP single quantum well. Photoluminescence originating from the GaInP barrier layer, the quantum well (E1) and the GaAs buffer are labeled.
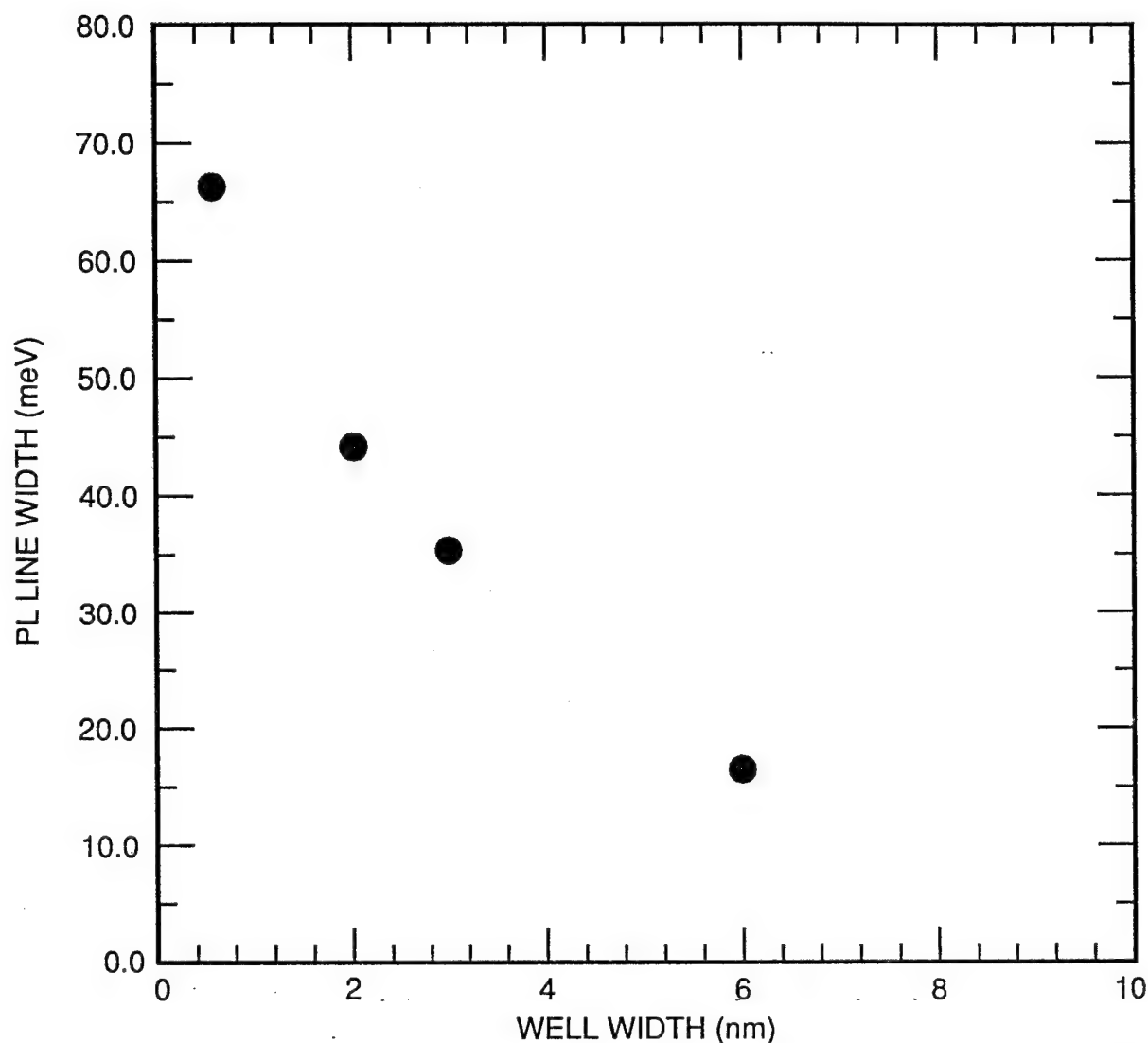
Figure 2.14. Photoluminescence line width versus well width for ALE GaInP/GaAs/GaInP single quantum well.

2.4.3 AlGaAs Films

Thick AlGaAs films grown by ALE were studied by low-temperature PL. Shown in Figure 2.15 is the PL spectrum of an undoped $Al_xGa_{1-x}As$ film with an AlAs mole fraction of 0.28. As a figure of merit, the line width of the dominant AlGaAs PL band is 15 meV. For high-temperature (800° to 870°C) grown MBE AlGaAs,[24] PL line widths of less than 4 meV have been observed. However, PL line widths for AlGaAs grown by MBE at more standard growth temperatures (e.g., 600°C) are typically 12 to 25 meV FWHH for x between 0.20 and 0.30. Hence, the PL line width of these films is comparable to that of good MBE films. The ultimate film quality of ALE AlGaAs appears to be limited by growth temperature.

31
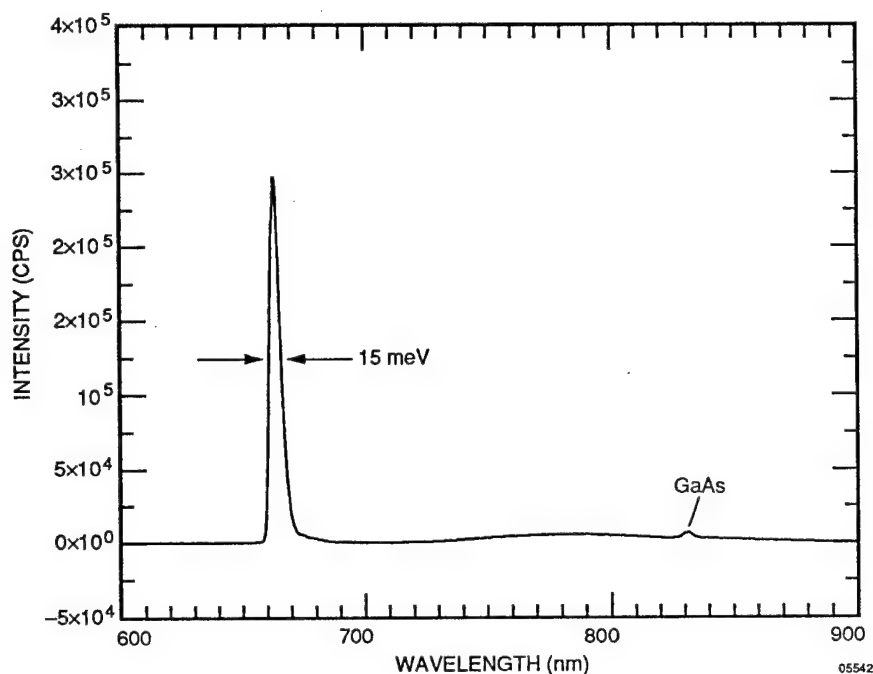
Figure 2.15. Low-temperature (4.2 K) photoluminescence spectrum of high-purity ALE AlGaAs. A weak feature caused by the GaAs substrate is also observed.

A stack of three single AlGaAs/GaAs quantum wells was studied at 4.2 K by PL. The quantum wells were nominally 1.4, 2.0, and 8.4 nm thick, and each well was separated by 100 nm of ALE-grown AlGaAs. The composition of AlGaAs was 0.28. The photoluminescence spectrum of this stack of single quantum wells is shown in Figure 2.16. For comparison, the PL full-width versus well-width behavior of MBE-grown quantum wells is presented in the figure. The FWHH maximum of the 14-nm well is about 7.1 meV, indicating the excellent quality of these structures. The full widths of the 2.0- and 8.4-nm wells are 0.56 and 0.54 nm respectively, showing very little carrier broadening. A comparison between ALE and MBE quantum-well PL full widths is presented in Figure 2.17. These results show that the ALE wells are more abrupt and exhibit less carrier broadening than comparable structures grown by MBE. Additional properties of these ALE AlGaAs films are presented in Reference 7.

2.4.4 GaP and GaAsP

Several quantum-well structures using GaP or GaAsP as barrier material were grown and studied. Clear optical evidence of quantum confinement was observed only in the GaAsP/GaAs/GaAsP structures. The low-temperature PL spectrum of a GaAsP/GaAs/GaAsP well is presented in Figure 2.18. This structure contained 50-nm GaAsP barrier layers and a 6-nm GaAs well. The full width of the well luminescence is 14.9 meV. Although the theoretical PL line-width versus well-width behavior is not available for this system, these experimental results show that quantum confinement can be obtained with the GaAsP/GaAs system grown by ALE.
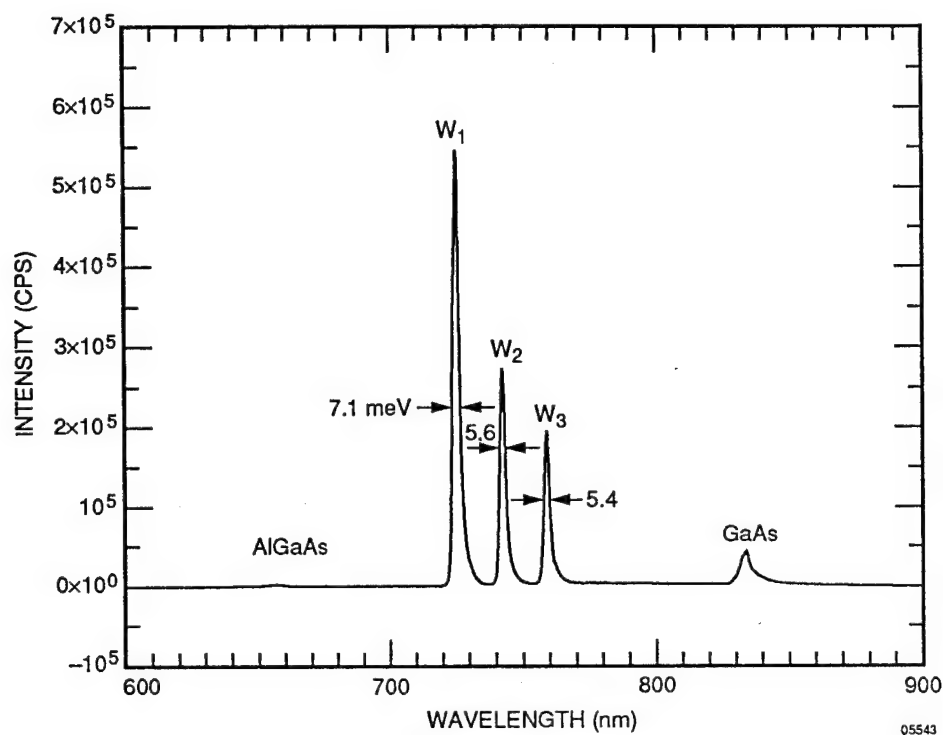
32

Figure 2.16. Low-temperature (4.2 K) photoluminescence spectrum of stack of single quantum wells. Photoluminescence from the AlGaAs barrier layer, the three isolated quantum wells (W1, W2, W3), and the GaAs buffer are evident.
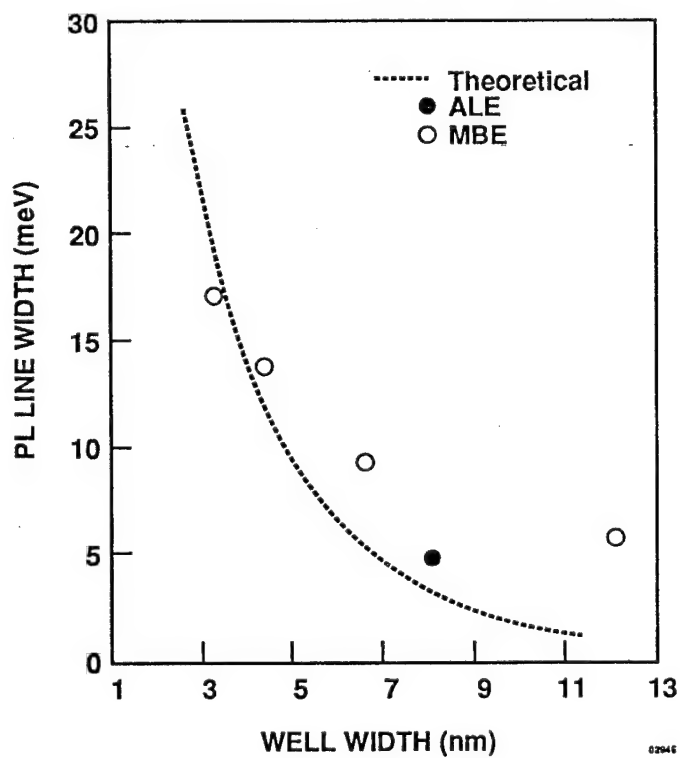
Figure 2.17. Photoluminescence line width from ALE and MBE quantum wells at 4.2 K.

33
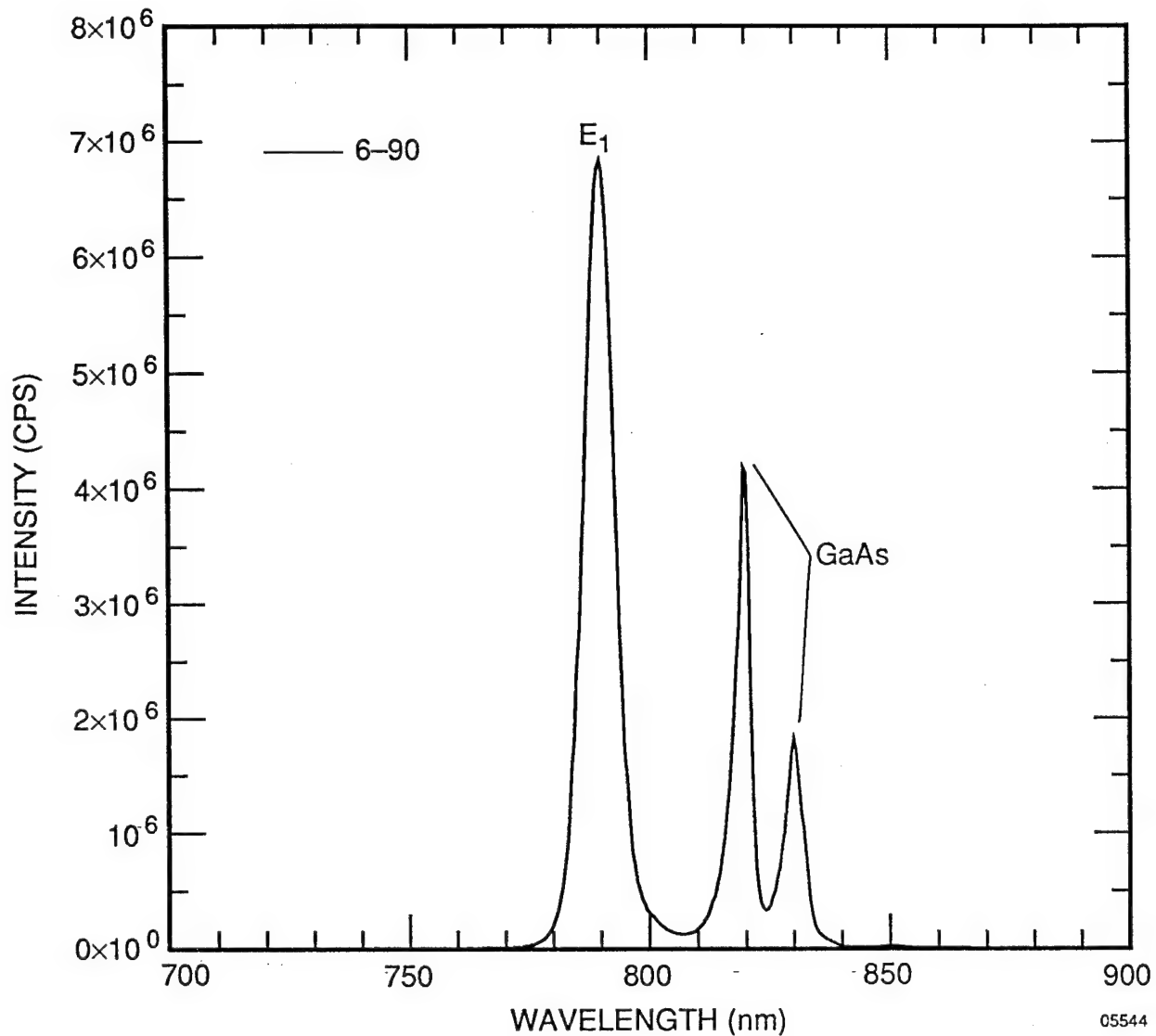
Figure 2.18. Photoluminescence spectrum at 4.2 K of GaAsP/GaAs/GaAsP single quantum well. Features caused by the quantum well E1 and the underlying GaAs are observed.

In summary, we have fabricated and characterized several advanced electron device structures grown by atomic-layer epitaxy. The results of the first ALE pnp HBTs, delta-doped FETs, and RTDs are reported. Further development of the ALE growth method is indicated to exploit the unique capabilities of ALE over conventional MBE and MOMBE systems.

3-Dynamic Content Adressable Memory

A content addressable memory (CAM) is a data storage medium that can be accessed by searching for specific data content. One has the choice of using a six transistor static random access memory (SCAM) or a two transistor dynamic random access memory (DCAM) as the storage units in a CAM. The advantage of the DCAM is a smaller size for the storage element and less power dissipation than with the SCAM. The disadvantages of the DCAM is that the data has to be periodically refreshed and typically reading the cell destroys the stored data unless some form of non-destructive readout is used; otherwise the data must be read and then written back into the cell. In this section we first demonstrate GaAs DRAM cells using JFET- and MESFET-access transistors. Then a 2x2 GaAs DCAM array is demonstrated based on a JFET-access DRAM cell. Finally, trench storage capacitors are demonstrated whose use would lead to increase charge storage density in the DCAM.

3.1 JFET-Acessed DRAM Cell

The epitaxial common N-channel JFET-accessed GaAs DRAM cell is pictured in Fig. 3.1. The N epilayer provides the channel of the access transistor as well as the N-type storage node of the P^+N junction capacitor. The physical layout of the cell is given in Fig. 3.2. This structure consists of two 100 x 300 μm^2 P^+N junction storage capacitors surrounded by a ring-gate JFET access transistor with $L_{Gate} = 5 \mu m$. Although only one contact is needed to form a bitline connection, a source and drain contact were included to test the characteristics of the access transistor.

The charge state of the storage node is determined by measuring the capacitance between the two P^+ capacitor plates. Unless otherwise specified, the capacitor plates are held at system ground along with the substrate. When the N-region of the storage capacitor is at zero bias, the equilibrium depletion capacitance of the two storage capacitor plates in series is observed representing a logic zero state. When the N-region has been charged to a positive potential representing the logic one state, the reverse bias on the diode junctions result in a lower measured depletion capacitance.
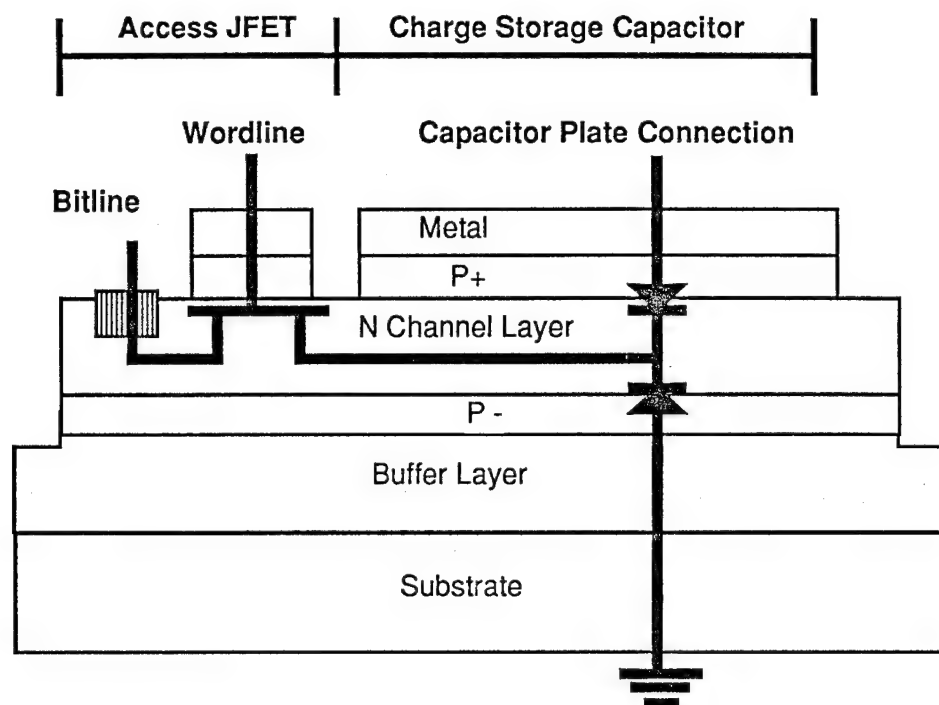
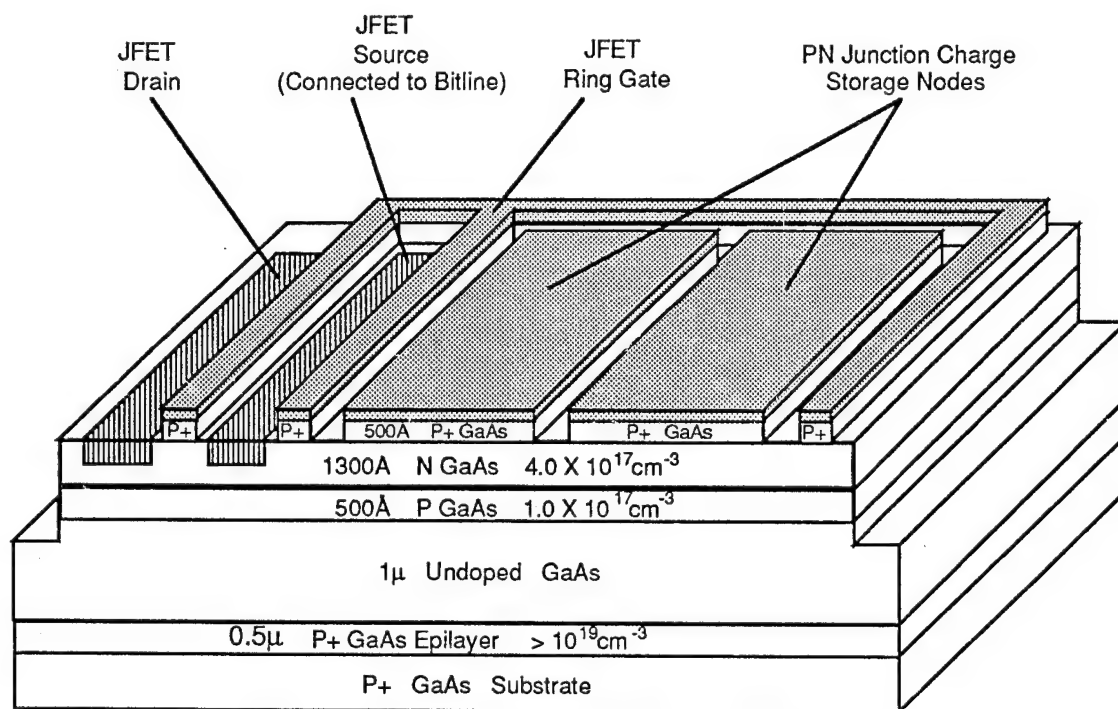Fig.3.1   Common N-channel epitaxial JFET-accessed GaAs DRAM cell.

Fig.3.2 Physical realization of the first reported GaAs JFET-accessed 1-T DRAM cell.

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To write a logic one, the bitline is taken to V_{high} = 0.7 V and the access transistor is turned on by taking the gate to $V_{WL(on)}$ = 0 V. Electrons flow from the storage node to the bit-line contact through the turned-on access transistor charging the N storage node to a positive potential. The write cycle is completed by restoring the wordline to $V_{WL(off)}$ = -1.5 V prior to the bitline voltage changing from V_{high}. A logic zero is written to the cell in the same manner, except the bitline is held at V_{low} = 0 V instead of V_{high}.

Fig. 3.3 shows an experimental demonstration of this writing of 1's and 0's to the cell. Data are strobed into the cell during 1-ms write pulses applied to the gate of the access transistor. The measured capacitance changes at the time the write pulse is applied, indicating a proper change in the charge-state of the storage node. The fact that the capacitance does not change when the bitline voltage is altered shows that the bitline is sufficiently isolated from the storage node by the turned-off access transistor.

Reading of stored information is demonstrated in Fig. 3.4. Here the bit line is monitored by a 0.5 pF active probe. With the access transistor turned off by V_G = $V_{WL(off)}$ = -1.45 V, electrons are removed from the storage node by forward biasing the top capacitor plate junction with a positive bias pulse to pseudo-write a logic one. A short time later the charge state of the cell is sampled by bringing V_G = $V_{WL(on)}$ = 0 V to turn on the access transistor connecting the storage node to the bitline. A positive voltage excursion is observed on the bitline as the active probe charge shares with the positively charged storage capacitor. The bit-line voltage decays in about 250 µs due to leakage through the shunt resistance of the probe (Fig. 3.4), and this discharges both the probe tip and the storage capacitor. A second read pulse at 3.5 ms shows a much smaller voltage excursion because the storage capacitor was discharged by the previous read operation and now contains a logic zero. The small excursion while reading the logic zero is attributed to charge redistribution during the positive voltage swing of V_G, as some electrons flow from the bitline to fill the shrinking gate depletion region. In a complete integrated circuit implementation, sense amplifiers would account for this in detecting and latching the data for readout.
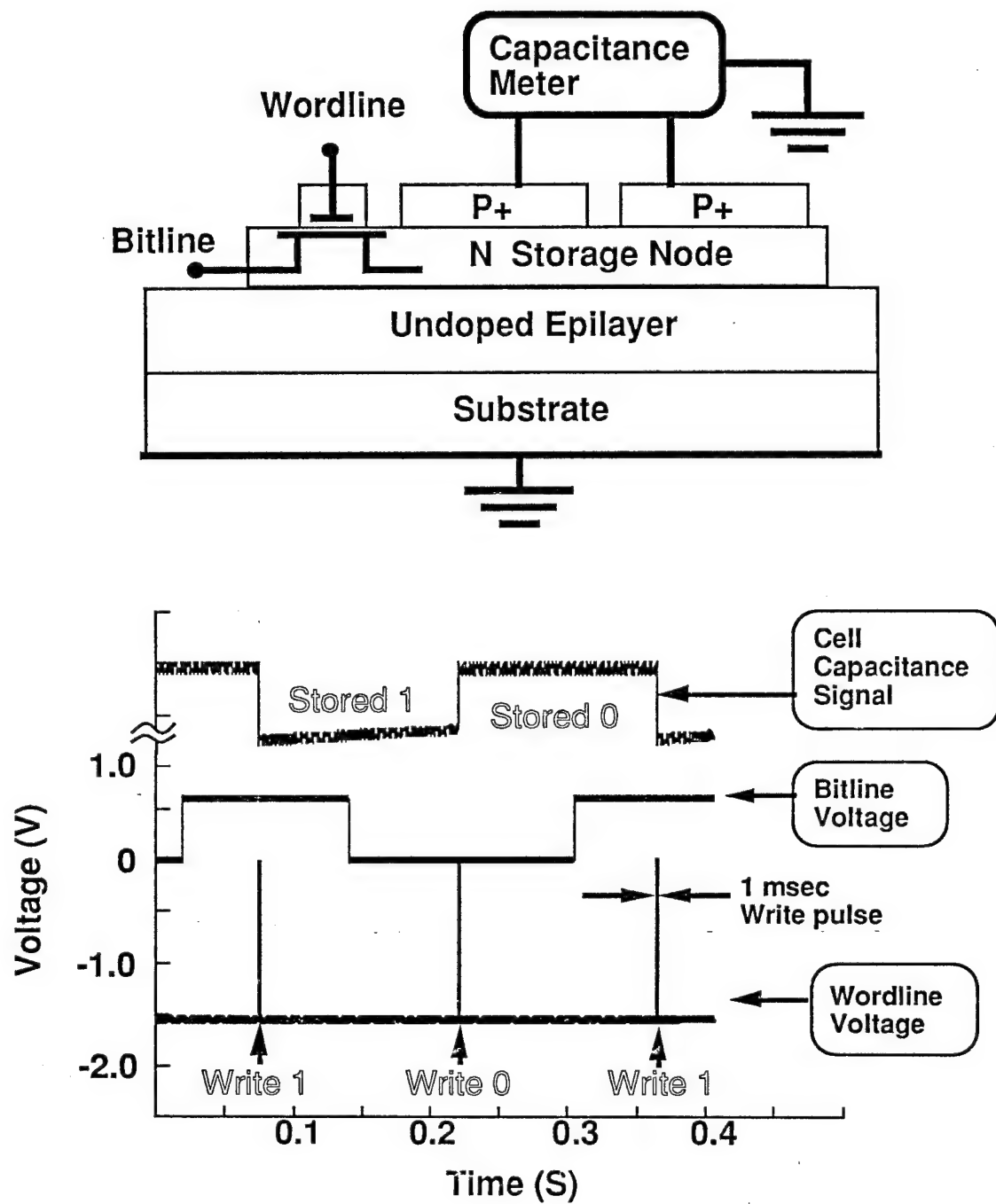
Fig. 3.3   Demonstration of the write capability of the JFET DRAM cell. Note that the capacitance changes at the time of the 1-ms wordline (gate) pulse in accordance with the voltage applied to the bitline contact. This data was taken at room temperature in the dark on the DRAM cell of Fig.3.2.

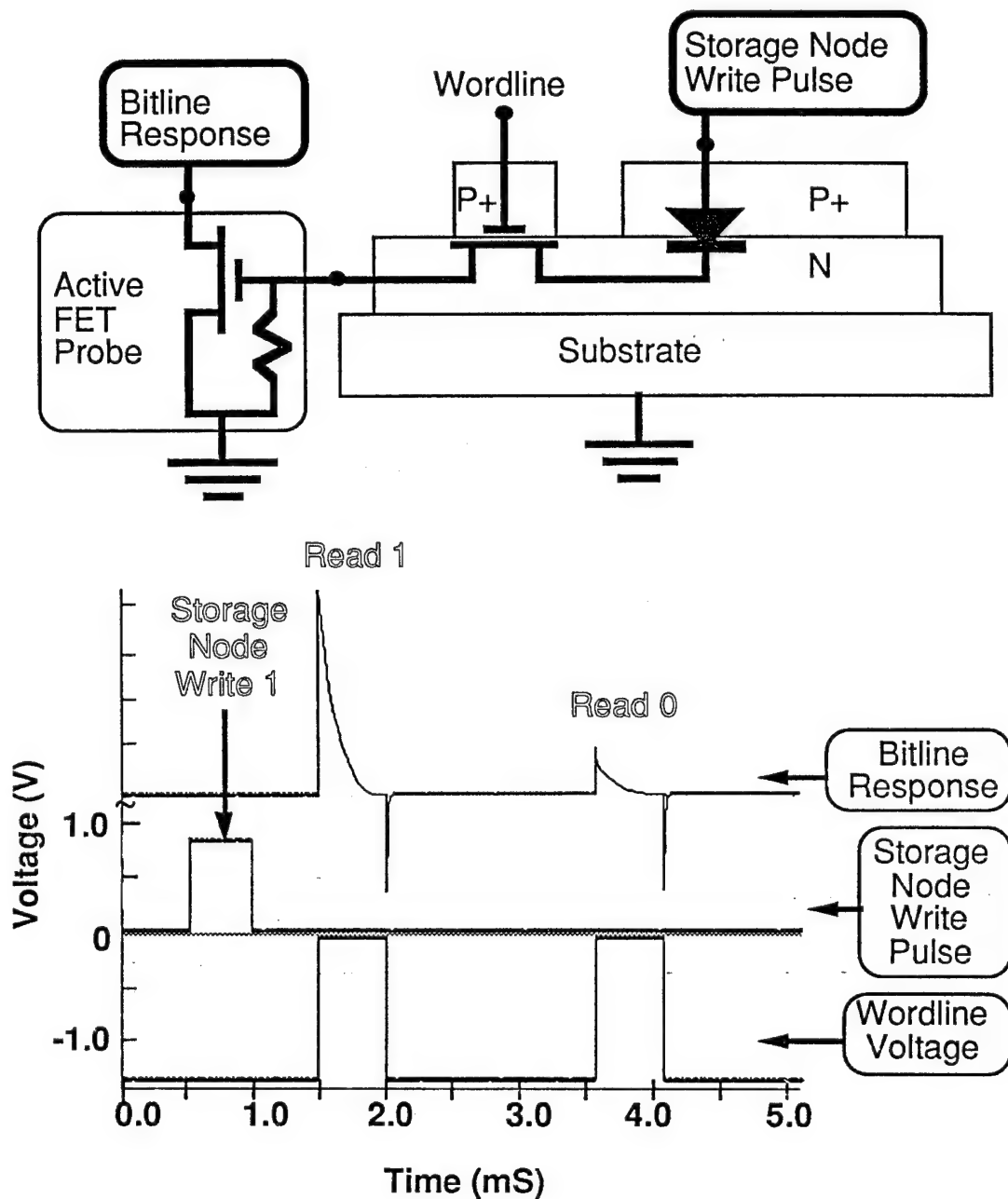Fig. 3.4   Demonstration of the read capability of the JFET DRAM cell. The potential of the bitline is monitored by a 0.5 pF active probe, which electrically behaves like a DRAM array bitline during a sense cycle. See text for further explanation.

3.2 MESFET-Accessed DRAM Cells

Fig. 3.5 shows a cross-section of the recess-etched epitaxial MESFET DRAM cells that were investigated. The cell features a MESFET-access transistor directly connected to a P^+iN^+ storage capacitor. One of the main advantages of this configuration over the JFET configuration is that the N-layer profiles of the access transistor and storage capacitor can be optimized separately. The charge density and available logic swing of the storage capacitor are maximized by the heavily-doped N^+ layer, while the threshold voltage of the access transistor can be set independently by the depth of the recess-etch.

The MESFET-accessed cell is read and written in the same manner as the JFET-accessed cell of the previous section. The only change is that the operating voltages must be adjusted to match the I_D versus V_{GS} characteristics of the MESFET's in question. Fig. 3.6 demonstrates the write operation of a MESFET-accessed DRAM cell, whereby the writing of 1's and 0's to the cell is monitored by measuring the storage node capacitance. An active-probe measurement, similar to what was carried out on the JFET cell, verified the read operation of MESFET-accessed DRAM cells as shown in Fig. 3.7.

$(NH_4)_2S$-Treated MESFET DRAM Cell

The storage times for the MESFET-accessed DRAM cells were much shorter than the JFET-accessed DRAM cells. (Tens of milliseconds for the MESFET-accessed DRAM cell as opposed to seconds for the JFET-accessed DRAM cells.) This was caused by the large gate-to-drain leakage currents due to the low Schottky barrier height of the gate of the MESFET. An $(NH_4)_2S$-treatment before metallization, which increases the Schottky barrier height of the gate, was incorporated in a fabrication run of MESFET-accessed DRAM cells. Fig. 3.8 illustrates the increase in storage time observed on the non-ring-gate structures. Following the writing of a logic one to the cell, the untreated cell decays to the 1/e point in 21 msec while the $(NH_4)_2S$-treated DRAM cell has a storage time of one second. This dramatic increase in storage time, due to decreased MESFET Schottky gate leakage, appears to be permanent as the devices have not degraded over the period of one year's storage in ordinary room air.
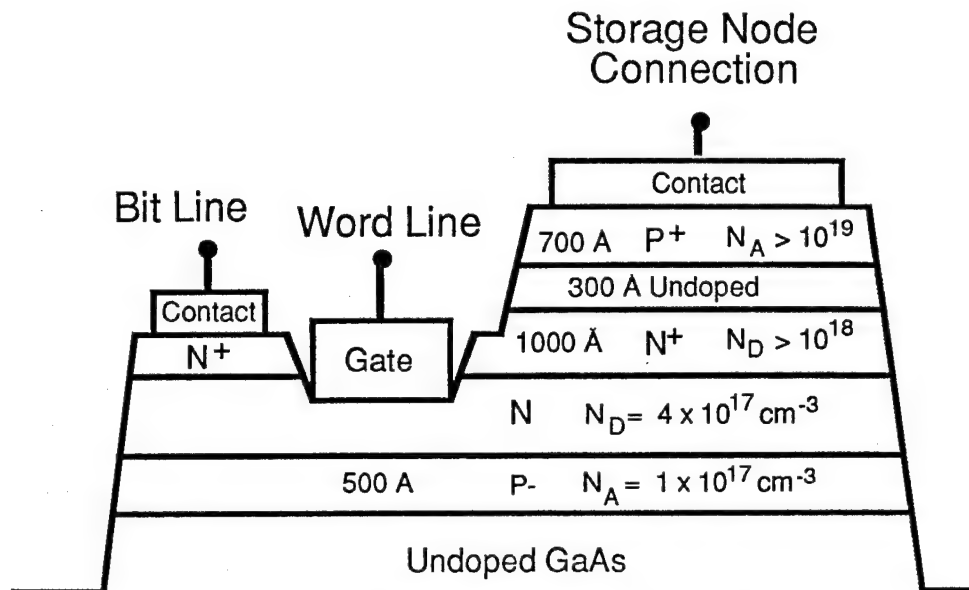
Fig.3.5   Recess-etched epitaxial MESFET DRAM cell. The thickness of the
N-channel beneath the gate is set by a recess etch. The target
thickness was approximately 800 Å, but there was deviation that was
witnessed by threshold voltage variations between wafer lots.
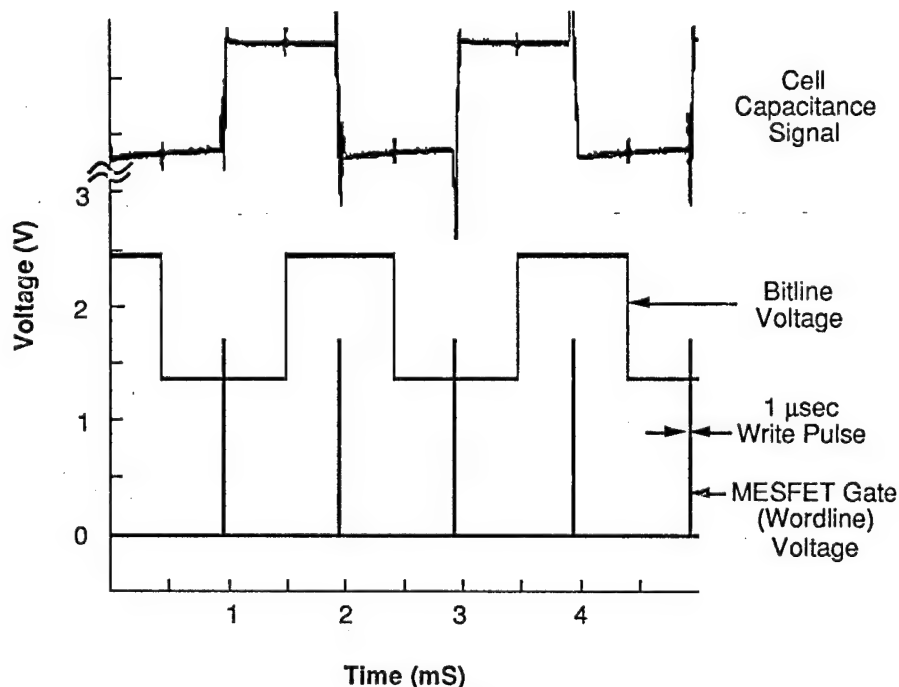
Fig.3.6   Demonstration of the write capability of an epitaxial MESFET DRAM cell.
The layout of this DRAM cell is the 10 x 200 μm^2 non ring-gate geometry.

4 1
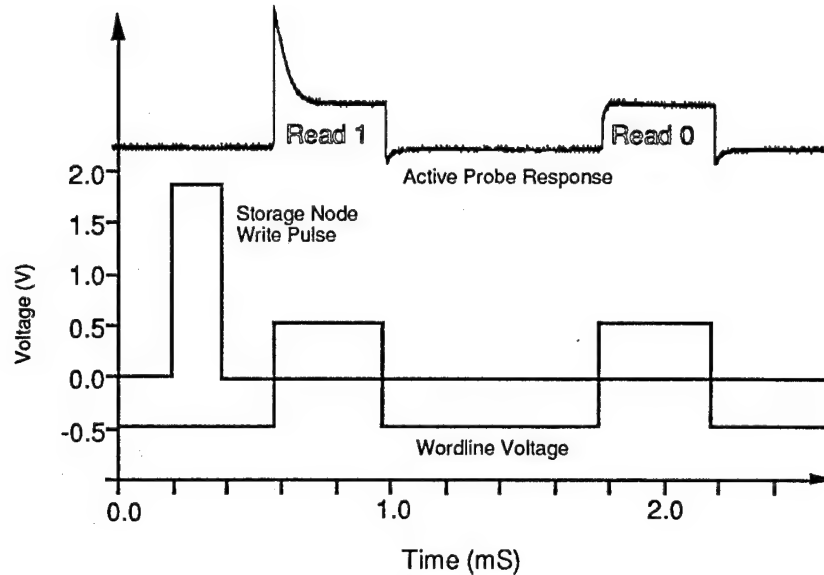
Fig. 3.7   Demonstration of the read capability of an epitaxial MESFET-accessed DRAM cell. The potential of the bitline is monitored by a 0.5 pF active probe, which electrically behaves like a DRAM array bitline during a sense cycle. The positive bitline excursion for the read 0 cycle is due to current drawn by the forward-biased Schottky gate.
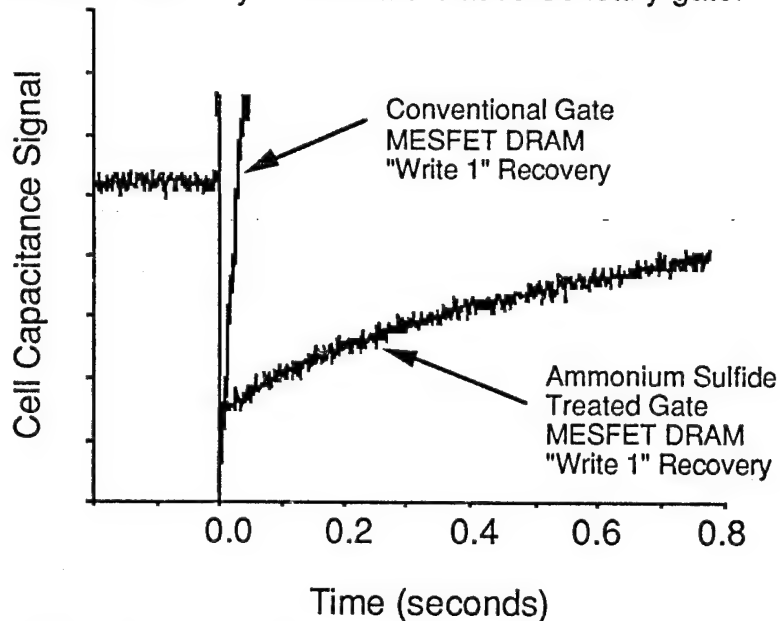
Fig 3.8   Comparison of write one recovery transients between conventional gate and $(NH_4)_2S$-treated gate MESFET DRAM cells.

3.3 Common N-Channel JFET DCAM Cell

To incorporate one-transistor dynamic RAM technology into a GaAs CAM, the dynamic content addressable memory (DCAM) cell of Fig. 3.9 was developed. The cell consists of two 1-transistor DRAM cells (to store the information and its complement) and a four-transistor XNOR gate for comparing the cell contents to keyword data on the bitlines. The DRAM part of the cell is based on the previously proven epitaxial JFET cell, and was chosen for its reliable simplicity.

Figure 3.10 depicts the layout of a single DCAM cell. The capacitors were made large to insure the presence of a large bitline signal during reading. The wordline and the matchline run horizontally parallel to each other through the middle of the cell on first level (gate) metal, while the bitlines and voltage supplies run vertically on the top level interconnect. The XNOR V_{SS} line along the left and right cell borders are shared with adjacent CAM cells in the array. For the voltage stored on the capacitor to gate the XNOR, an alloy contact to the storage node is needed. This contact is kept as small as possible to reduce any storage time degradation that the contact might cause.
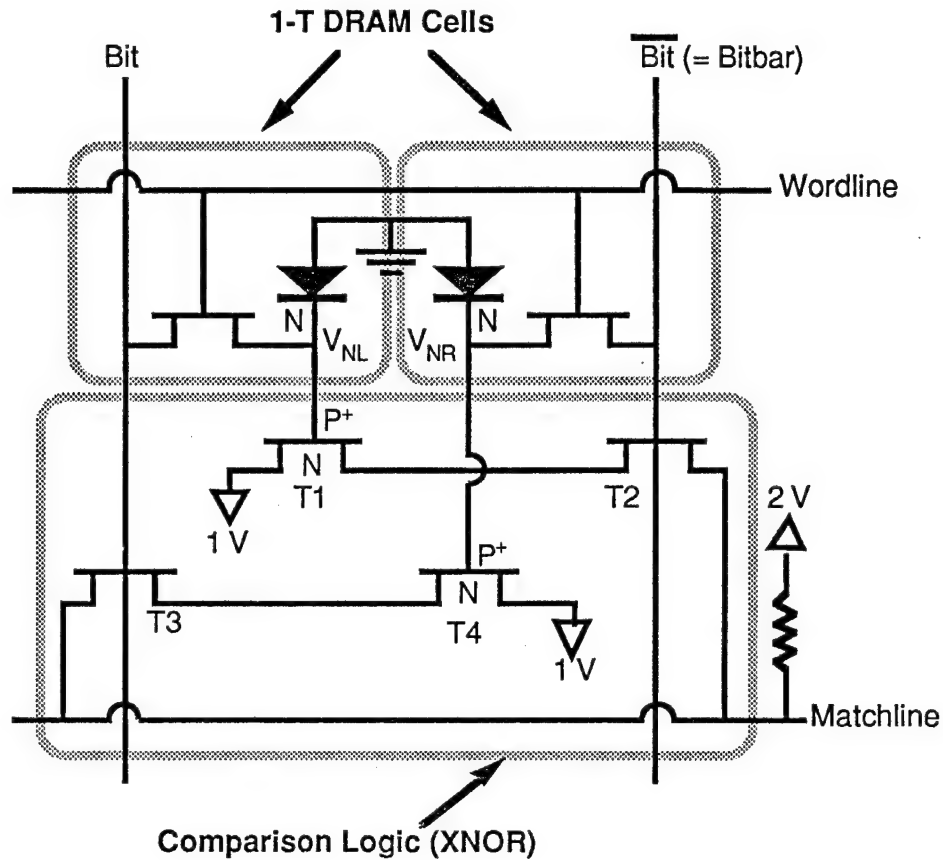
The mask set was divided into four different chips. The first three chips contained different-sized versions of the 2 x 2 DCAM array. The smaller tolerance arrays were made from scaled (half-sized and quarter-sized) copies of the largest tolerance array. The layout of the largest tolerance 2 x 2 array is shown in Figure 3.11, and the design rules used are evident in Figure 3.10. The array required 19 wire bond pads, which were 100 x 100 μm^2 with 50 μm spacing. The fourth chip, as well as leftover space on the first three chips, contained a wide variety of test structures. These test structures included various sizes and geometries of isolated storage capacitors, MESFET- and JFET-accessed DRAM cells, DCAM cells, and process testers. The devices were fabricated on approximately 1-inch square wafers.

Following diamond-scribe assisted breakup of the wafer, an individual die containing a full-sized 2 x 2 DCAM array was mounted into a 24-pin DIP package and wire bonded for testing. Functional testing of the array was carried out using a Tektronix 9100 Digital Analysis System (DAS), a Test Systems Strategies LFS-2 test stand, and a Tektronix 11401 Digitizing Oscilloscope. The DAS provided the programmable control signals necessary to drive the array, while the test stand provided a custom interface between the DAS and the 24-pin DIP socket. The digitizing oscilloscope recorded input and output waveforms. Control signals were routed from the DAS through the test stand to the 24-pin DIP socket using a wire-

1-T DRAM Cells

Bit   Bit (= Bitbar)

Wordline

V_{NL} V_{NR}

N   P+   T1   1 V   T2   2 V

P+   N   T3   T4   1 V

Matchline

Comparison Logic (XNOR)

Contents		Keyword		XNOR Transistors				Match	
V_{NL}	V_{NR}	V_{Bit}	V_{Bitbar}					$V_{Matchline}$	
(V)	(V)	(V)	(V)	T1	T2	T3	T4	(V)	
0	1	0	1	OFF	ON	OFF	ON	2	
0	1	1	0	OFF	OFF	ON	ON	1	
0	1	0	0	OFF	OFF	OFF	ON	2	
1	0	0	1	ON	ON	OFF	OFF	1	
1	0	1	0	ON	OFF	ON	OFF	2	
1	0	0	0	ON	OFF	OFF	OFF	2	

Fig. 3.9   JFET GaAs dynamic CAM cell and Electrical truth table demonstrating the operation of the DCAM cell comparison logic circuitry.. The data contents are stored in two 1-transistor JFET-accessed GaAs DRAM cells, and comparison operations are performed with the XNOR logic (see Table). All the transistors are depletion-mode epitaxial JFET's with $V_{T0} = -1.0$ V.

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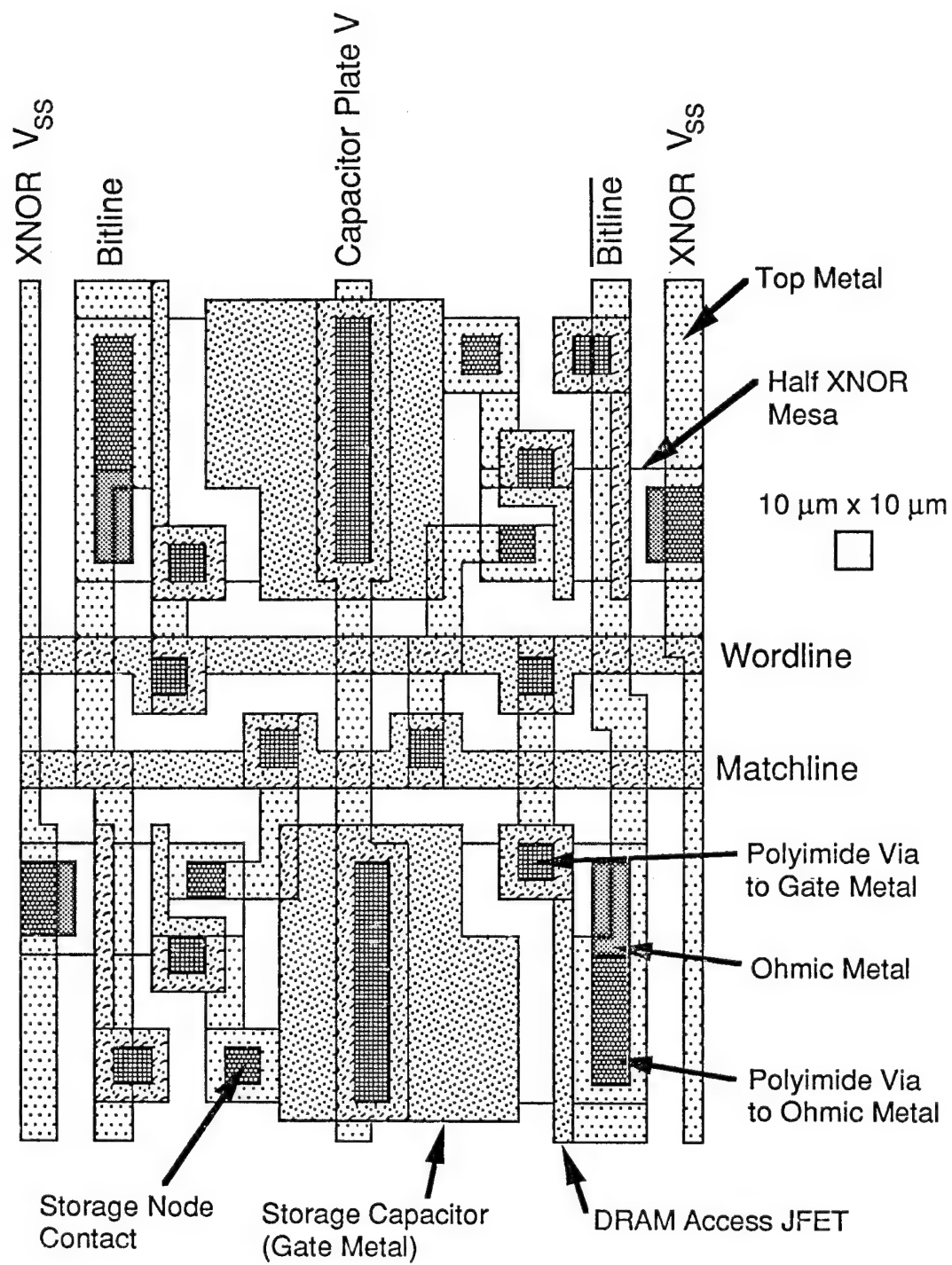
Fig. 3.10   Epitaxial GaAs JFET DCAM cell layout.

XNOR V$_{SS}$

Bitline

Capacitor Plate V

Bitline

XNOR V$_{SS}$

Top Metal

Half XNOR Mesa

10 μm x 10 μm

Wordline

Matchline

Polyimide Via to Gate Metal

Ohmic Metal

Polyimide Via to Ohmic Metal

Storage Node Contact

Storage Capacitor (Gate Metal)
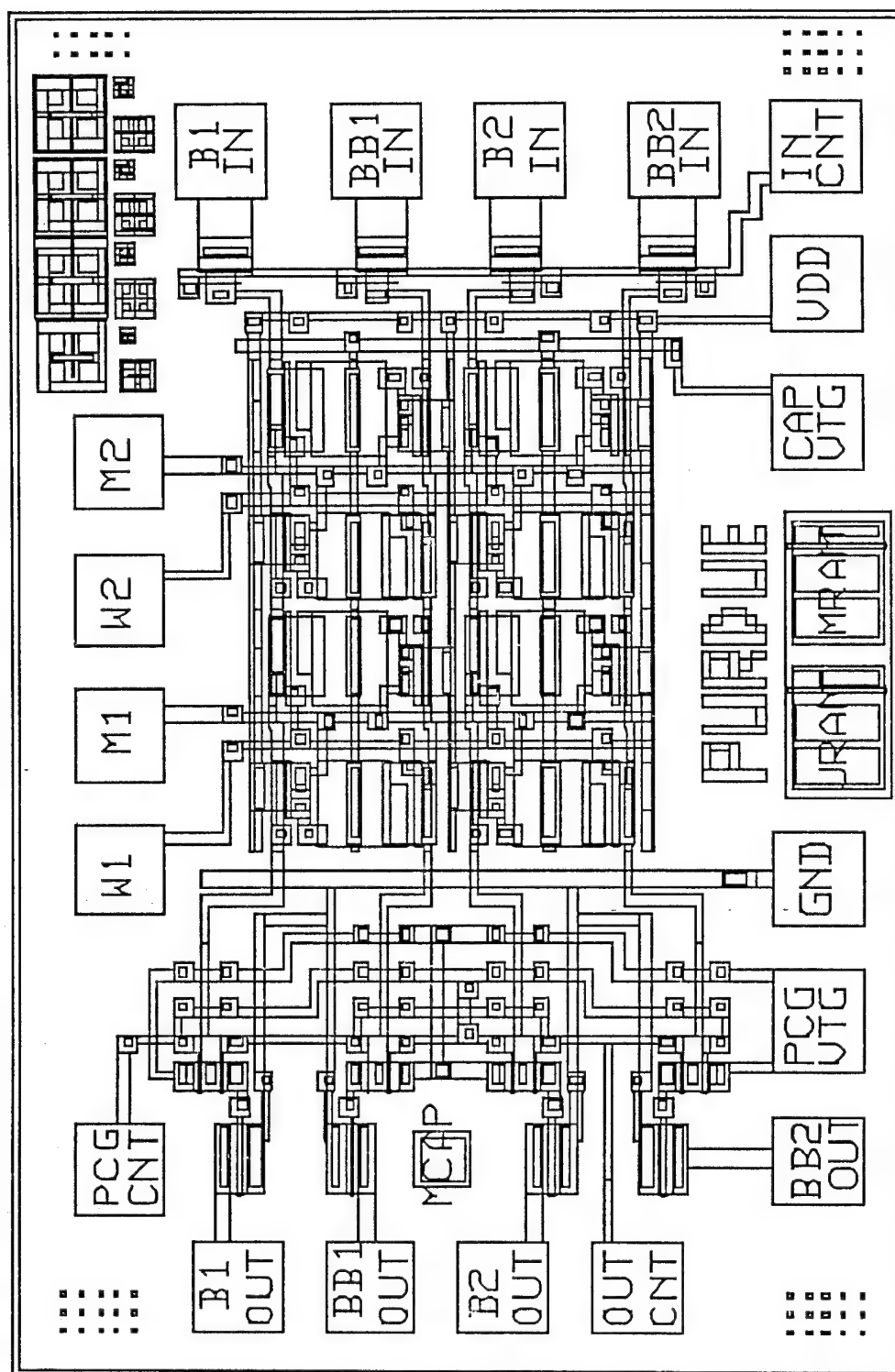
DRAM Access JFET

45

Fig. 3.11   Full-size 2 x 2 DCAM array test chip.

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wrapped configuration board. The wiring custom-built for testing the DCAM array provided slots for measuring and supplying voltages, and included adjustable output pull-up resistors. The control signal pattern (i.e., 1's and 0's) is set by programming the DAS, but the operating voltages seen by the chip are set by external DC supplies which power various output busses on the test stand.

The functional characterization of the DCAM array was divided into two parts. The first concern was to verify the proper operation of the GaAs DRAM array by writing, storing, and reading-back various test patterns. This is demonstrated by the measured waveforms of Fig. 3.12 and 3.13. In order to understand these waveforms, it is useful to recognize that the 2 x 2 DCAM array is now being operated as a 4 x 4 DRAM array, with both input and output accomplished via the bitlines. Figure 3.12 is a blown-up portion of Fig. 3.13 that details the write-store-read test on the 4-bit input combination of all 0's. The captions along the top of Fig. 3.12 timing diagram annotate each step in the sequence. The test sequence starts by writing all 4 bits of memory, a 0 0 for the two bits in row W1 followed by another 0 0 for the two bits in row W2. Usually the precharge voltage is halfway between DRAM V_{high} and V_{low}, but to save on the number of power supplies needed for testing it was set to V_{high}. The successful read-back of the stored data can be witnessed by the response of the bitline OUT signals when the appropriate wordline goes high. This test sequence is repeated for various 4-bit test patterns in Fig. 3.13, and the array successfully passed all DRAM read/write test patterns. The unsharpness of the rising and falling edges of the waveforms is due to shortfalls in the testing setup, and does not reflect speed limitations in the array.

With proper data storage demonstrated, waveforms verifying the match read capability of the DCAM array are shown in Fig. 3.14. In a two-bit word where each digit could be a 0, 1, or d = "don't care", there are nine possible combinations that could be input as the keyword on the bitlines. These are shown in columns B1 and B2 in the truth tables across the top, and form a basis for performing 9 comparison read tests for each 4-bit data pattern that's stored in the array. The test sequence of Fig. 3.14 consists of writing a 4-bit pattern into the array (shown along the figure bottom), and then performing all 9 possible comparison read operations against the stored data. The truth tables across the figure top show the correct matchline outputs M1 & M2 for each keyword input when compared against the six different stored data combinations shown along the figure bottom. An inspection of the matchline and bitline waveforms reveals that the DCAM array functions correctly for all 54 combinations tested in Fig. 3.14.
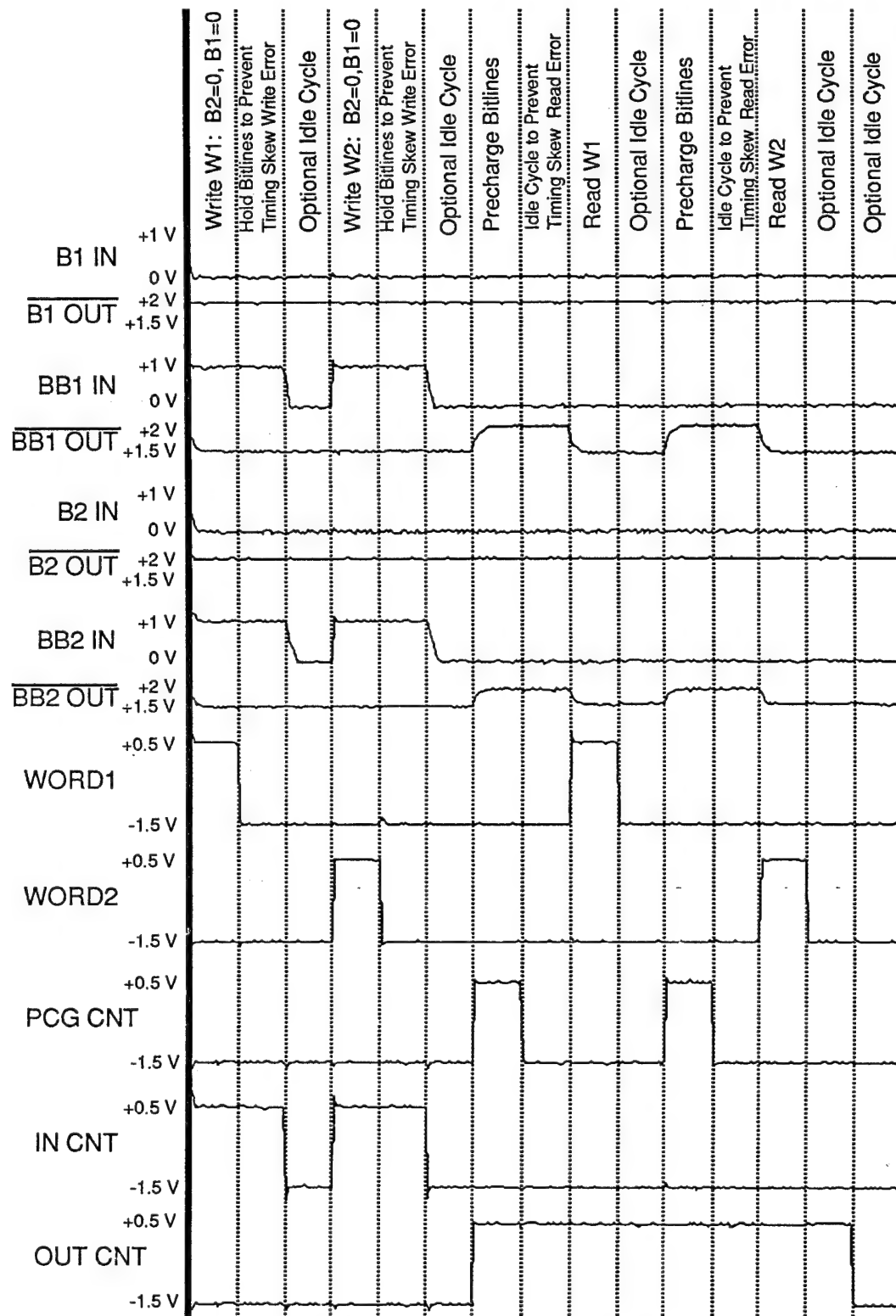
47

Fig. 3.12   Waveforms demonstrating the successful write and read of a 4-bit pattern
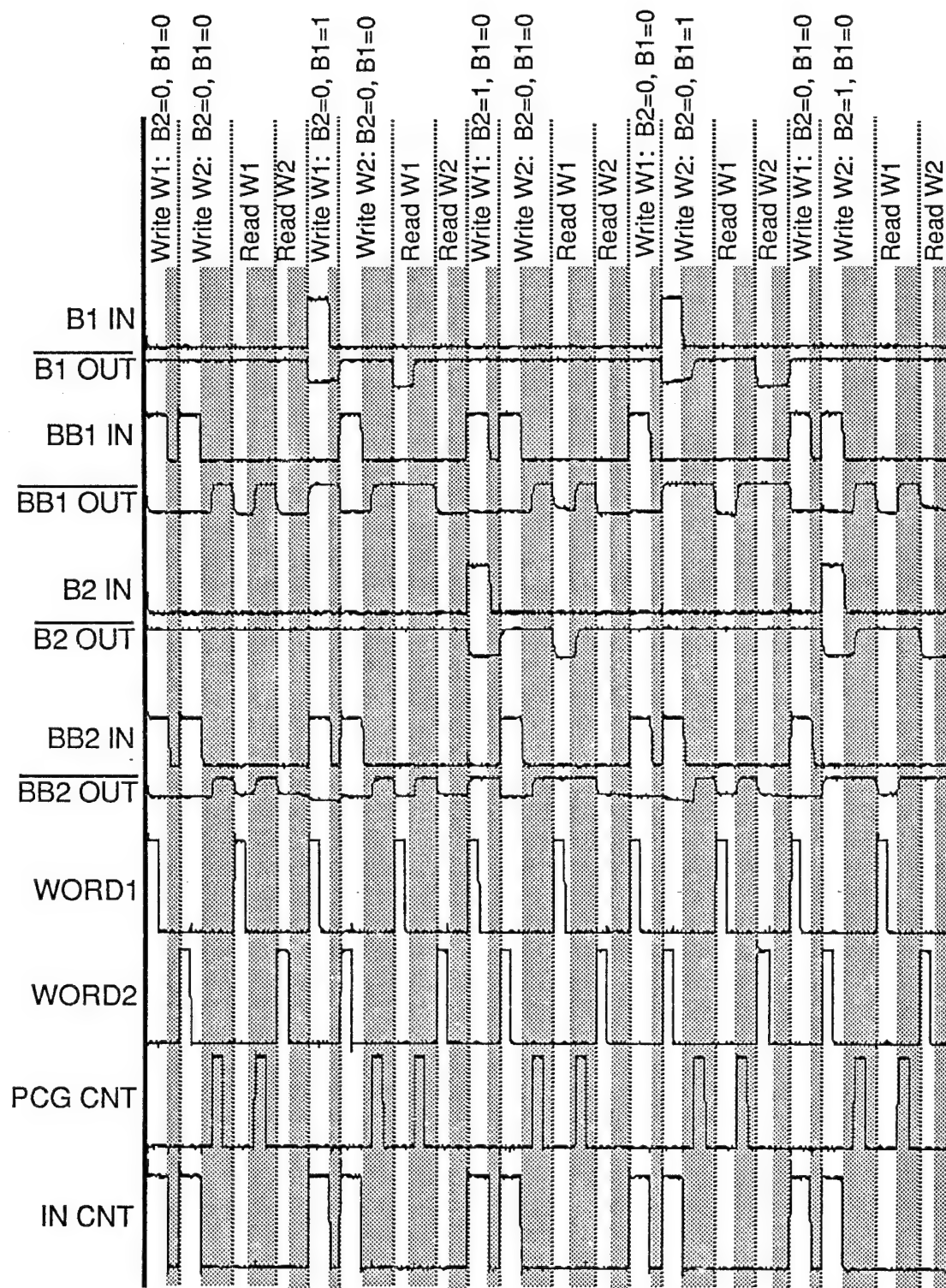of all zeros. Clock period = 100 µsec.

4 8

Fig. 3.13   Waveforms demonstrating successful write and read operation of DCAM array for 5 input combinations. Clock = 100 μsec.

B2	B1	M1	M2
0	0	H	H
0	1	L	H
1	0	L	L
1	1	L	L
d	0	L	H
d	1	L	H
0	d	H	L
1	d	L	H
d	d	H	H

B2	B1	M1	M2
0	0	L	L
0	1	L	L
1	0	L	L
1	1	H	H
d	0	L	H
d	1	L	H
0	d	L	L
1	d	H	H
d	d	H	H

B2	B1	M1	M2
0	0	L	H
0	1	L	H
1	0	L	L
1	1	H	L
d	0	H	H
d	1	H	H
0	d	L	H
1	d	H	L
d	d	H	H

B2	B1	M1	M2
0	0	L	L
0	1	L	L
1	0	H	H
1	1	L	H
d	0	H	H
d	1	L	L
0	d	L	L
1	d	H	H
d	d	H	H

B2	B1	M1	M2
0	0	L	L
0	1	L	H
1	0	H	L
1	1	L	L
d	0	H	L
d	1	L	L
0	d	L	H
1	d	H	L
d	d	H	H

B2	B1	M1	M2
0	0	L	H
0	1	H	L
1	0	L	L
1	1	L	L
d	0	L	H
d	1	L	H
0	d	H	H
1	d	L	L
d	d	H	H

M1

M2

B1

BB1

B2

BB2

	B2	B1
W1	0	0
W2	0	0

	B2	B1
W1	1	1
W2	1	1

	B2	B1
W1	1	1
W2	0	0

	B2	B1
W1	1	0
W2	1	0

	B2	B1
W1	1	0
W2	0	1

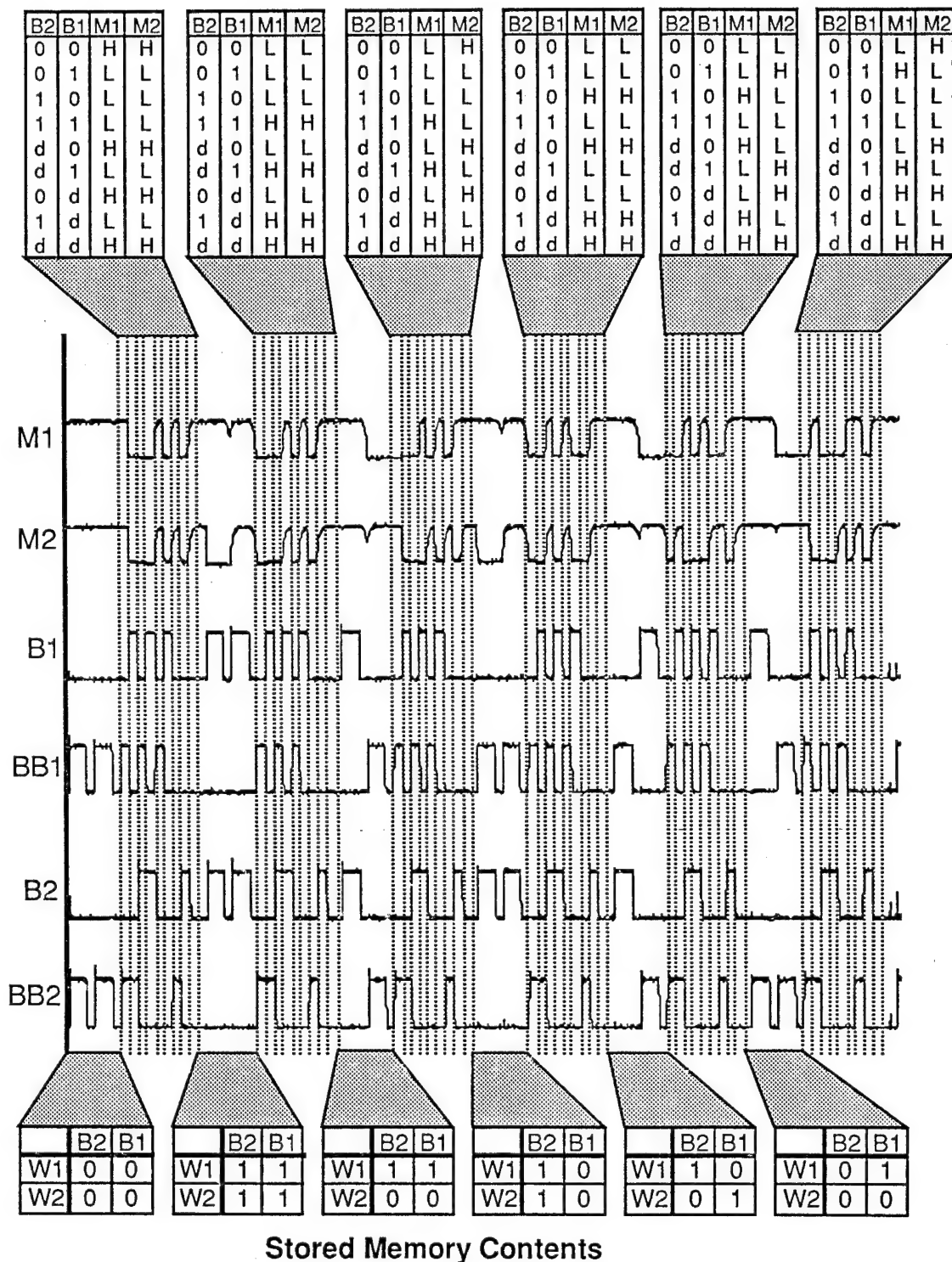|	B2	B1
W1	0	1
W2	0	0

Stored Memory Contents

Fig. 3.14   Waveforms verifying successful content addressable memory operation. Clock = 100 μsec.

3.4 Trenched Diodes Grown By Atomic Layer Epitaxy

Atomic layer epitaxy (ALE) is a growth technique that proceeds in a self-limiting fashion so that growth takes place on all crystal surfaces with greater uniformity. ALE has demonstrated a unique sidewall growth capability which could be exploited to produce epitaxial trenched PN junction storage capacitors. However, previous work regarding sidewall ALE has failed to address the electrical quality of the sidewall material. Therefore to characterize the electrical quality of ALE-grown sidewall material and to investigate this possibiltiy of trenched epitaxial PN junction storage capacitors, a study of PiN diodes grown by ALE in trenches and sidewalls was undertake. Many silicon DRAM cells employ trenched storage capacitor technologies to increase charge storage densities, so it is appropriate that this research investigated trenched PN junctions for use as GaAs storage capacitors.

PiN diode structures analagous to Fig. 3.15 were fabricated. The measured depth of the trenches was 2 μm. It should be noted that proper preparation of the substrate prior to growth is critical, as it seriously affects the quality of the subsequently-grown ALE material. Leakage currents due to the trenches were characterized using the three 100 x 100 μm diode structures. One diode has a planar top surface, one contains a single 30 x 30 x 2 μm trench (Fig. 3.15), and one contains nine 10 x 10 x 2 μm trenches. The total horizontal surface area is the same (10^4 μm^2) on each of the three diode mesas. Moreover, the horizontal area at the bottom of trenches is exactly 900 μm^2 on both the 1-trench and the 9-trench samples. The only difference between the 1-trench and 9-trench samples is the trench perimeter (which has a 3:1 ratio) and the number of trench corners (which has a 9:1 ratio). An independent test structure was used to verify that material in the bottom of the trenches is electrically connected to the top planar surfaces via the ALE-grown sidewalls.

At room temperature the reverse diode leakage currents were below the noise limit of conventional current measurement equipment, so I-V characterization was conducted at 144 °C. The I-V curves of the three 100 x 100 μm diodes are given in Fig. 3.16 along with the I-V curve of a 100 x 100 μm low-leakage diode which was fabricated on a planar substrate with no trenches. The nearly identical characteristics of the two planar diodes shows that excellent planar material was obtained on the trenched substrate. Planar devices fabricated entirely on the flat bottom surfaces of large trenches show the same leakage characteristics as planar devices on the top surface.
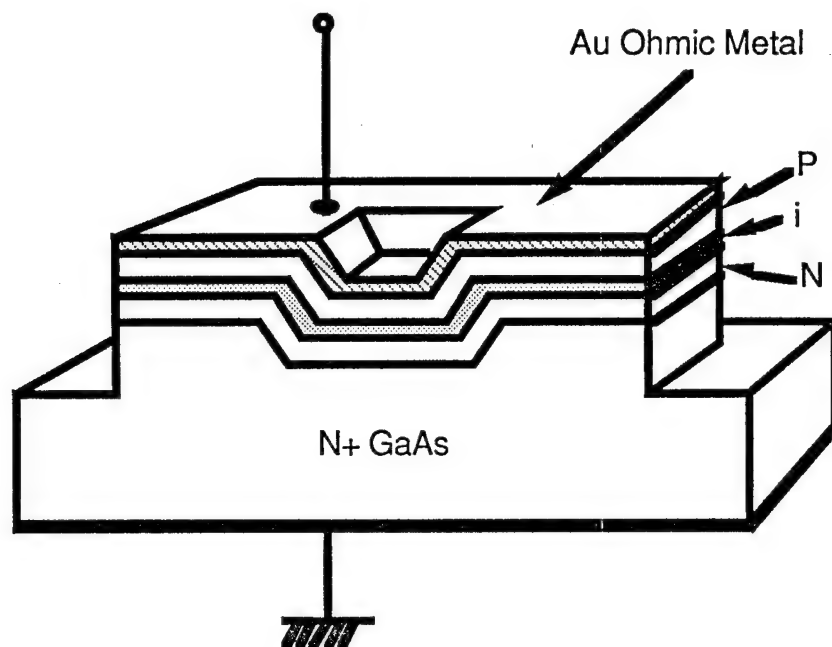
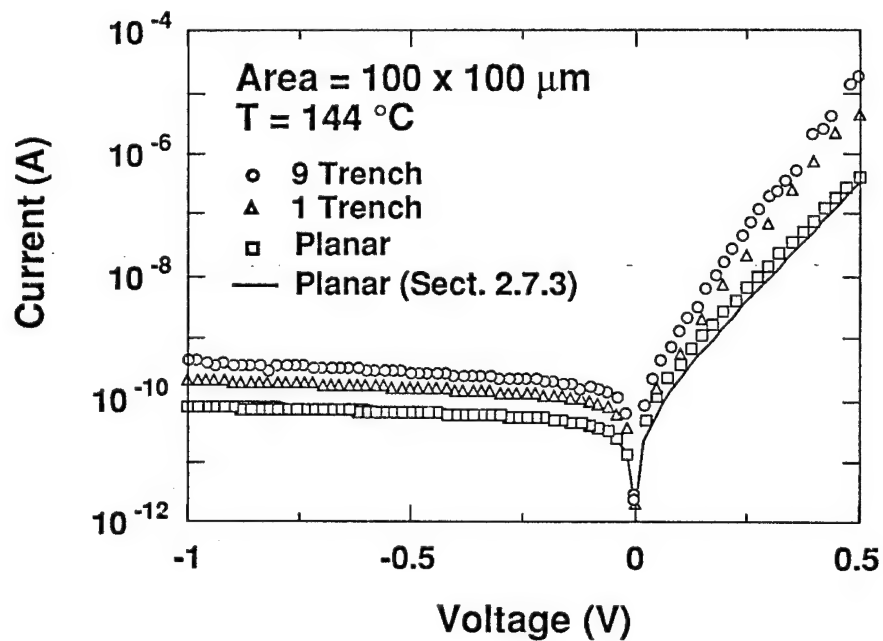Fig. 3.15   Schematic cross-section of a single-trench mesa-isolated PiN diode.

Fig. 3.16.   High temperature ALE PiN$^+$ diode I-V characteristics. The reverse current increases roughly as the square root of the voltage, indicating that thermal generation remains the dominant leakage mechanism.

Fig. 3.17 shows the dependence of leakage on trench perimeter for several devices of each type. A general linear dependence is apparent, indicating that sidewall leakage scales directly with trench perimeter and not with the number of trench corners. It is not possible from this data to determine whether sidewall leakage actually scales with sidewall perimeter or with sidewall area, since all trenches are the same depth. Further experiments are planned to determine the dependence on trench depth and on trench orientation. However, if the sidewall leakage component is normalized to sidewall area for these samples, we obtain a value of about 60 $\mu A/cm^2$ at 144 °C and 1 V reverse bias which is quite satisfactory for many device applications. However, this number is 60 to 100 times larger than the values obtained for comparable planar ALE diodes.

The reverse-bias sidewall current varies approximately as the square root of applied voltage, which suggests that thermal generation in the depletion region is the primary source of sidewall leakage. The temperature dependence of leakage current at 1 V reverse bias for the three 100 x 100 μm diodes is given in Fig. 3.18. The activation energy of leakage current on the 1-trench and 9-trench diodes are nearly the same, at 0.844 eV, while the activation energy of the planar sample is 0.713 eV.
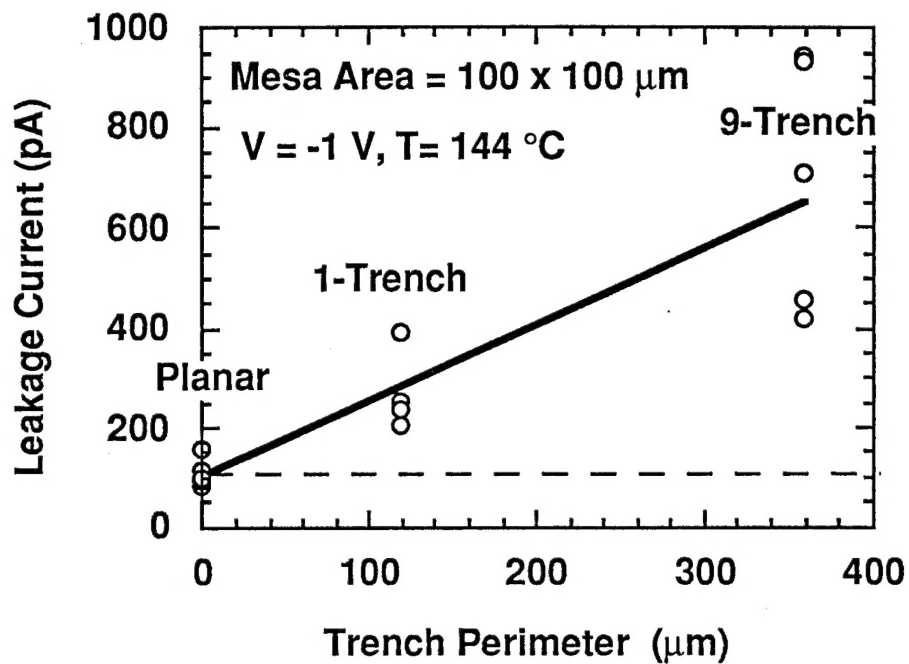
Fig. 3.17   Trench ALE leakage current as a function of trench perimeter.
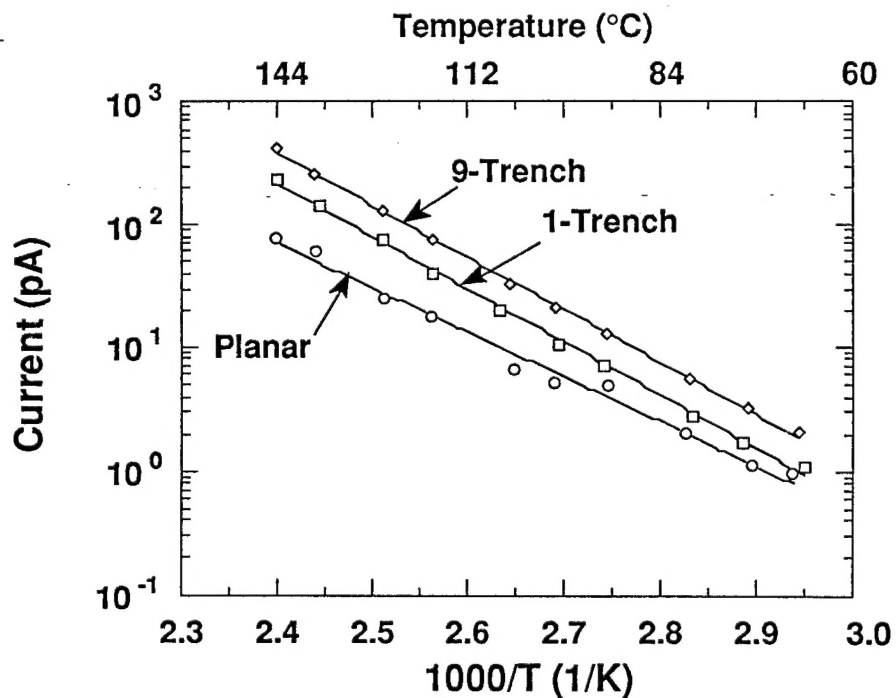

Fig. 3.18   Temperature performance of trench ALE diodes.

4. References

1. M. A. Tischler, and S. M. Bedair, edited by T. Suntola and M. Simpson, Chap. 4, Blackie and Son (1990).

2. S. M. Bedair, *Act a Polytechnica Scandinaviea* <u>195</u>, 17 (1990).

3. A. Usui and H. Sunakawa, *Jap. J. of Appl. Phys.* <u>25</u> (1986) L212-L214.

4. K. Mochizuki, M. Ozeki, K. Kodoma, and N. Ohtsuka, *J. Cryst. Growth* <u>93</u> (1988) 557-561.

5. P. C. Colter, S. A. Hussien, A. Dip, M. U. Erdogan, W. M. Duncan, and S. M. Bedair, *Appl. Phys. Lett.*, Vol. 59, p. 1440 (1991).

6. S. M. Bedair, M. A. Tischler, T. Katsuyama, and N. A. El-Masry, <u>47</u> (1985) 51-53.

7. J. R. Gong, P. C. Colter, D. Jung, S. A. Hussien, C. A. Parker, A. Dip, F. Hyuga, W. M. Duncan, and S. M. Bedair, *J. Crystal Growth*, Vol. 107, p. 83 (1990).

8. W. Jeong, E. Menu, P. D. Dapkus, *Appl. Phys. Lett.* <u>55</u> (1989) 244-246.

9. J. R. Gong, D. Jung, N. El-Masry, and S. M. Bedair, *Appl. Phys. Lett.* <u>57</u>, 400 (1990).

10. N. Kobayashi, T. Makimoto, Y. Yamauchi, and Y. Hovikoshi, *J. Appl. Phys.* <u>66</u> (1989) 640-651.

11. B. T. McDermott, K. G. Reid, N. A. El-Masry, S. M. Bedair, W. M. Duncan, X. Yin, and F. Pollak, *Appl. Phys. Lett.*, Vol. 56, p. 1172 (1990).

12. B. t. McDermott, K. Reid, N. El-Masry, and S. M. Bedair, *Mat. Res. Soc.* <u>160</u>, 355 (1990).

13. D. E. Aspenes, in Handbook on Semiconductors, Vol.2, edited by M. Bulkanski, North-Holland, New York (1980) p. 109.

14. A. Zunger, (private communications).

15. S. D. Hersee, E. Barbier, and R. Blondeau, *J. Crystal Growth* <u>77</u> (1986) 310-320.

16. K. Kamon, M. Shimazu, K. Kimura, M. Mihara, and M. Ishii, *J. Cryst. Growth* <u>77</u> (1986) 297-302.

17. M. Hashemi, J. Ramdani, B. T. McDermott, K. Reid, and S. M. Bedair, *Appl. Phys. Lett.* 56 (1990) 964-966.

18. /t. H. Chiu, J. E. Cunningham, B. Tell, and E. F. Schubert, *J. Appl. Phys.* 64 (1988) 1578-1580.

19. A. Usui, and H. Watanabe, Third International Conference on Modulated Semiconductor Structures, Montpellier, France (1987).

20. T. Henderson, B. Bayraktaroglu, S. Hussien, A. Dip, P. Colter, and S. M. Bedair, *Electronics Lett.*, Vol. 27, p. 692 (1991).

21. J. H. Luscombe and W. R. Frensley, *Nanotechnology*, Vol. 1, p. 131 (1990).

22. E. W. Williams and H. B. Bebb, in *Semiconductors and Semimetals*, edited by R. K. Willardson and A. C. Beer (Academic Press, New York, 1972), Vol. 8, p. 321.

23. H. Kunzel and K. Ploog, *Appl. Phys. Lett.*, Vol. 37, p. 416 (1980).

24. J. E. Cunningham, W. T. Tsang, T. H. Chiu, and E. F. Schubert, *Appl. Phys. Lett.*, Vol. 50, p. 769 (1987).

5. Ph.D. Completed Theses

- Philip G. Neudeck, PhD. May 1991, "Development, Demonstration, and Device Physics of FET-Accessed One-Transistor GaAs Dynamic Memory Technologies."

- Scott T. Sheppard, MSEE August 1991, "Characterization of Generation Mechanisms in Gallium Arsenide PiN Diodes."

- Brian McDermott, 1990, "Application of Atomic Layer Epitaxy to the Growth of III-V Compounds."

- Majid Hashemi, 1990, "Fabrication, Characterization, and Modeling of Non-alloyed FET Structures by ALE."

- Heng Liu, "Laser Assisted Growth of Optoelectronic Devices."